# PHYSIQUE DES COMPOSANTS SEMI-CONDUCTEURS

## X) FET et MOSFET: partie 1

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EPFL

# Historique du MOSFET

- **1926 – Concept du FET**

  J. Lilienfeld (US patent)

  …

  …

- **1960 – Premier MOS**

  D. Kahng (US patent)

- **1963 - Invention du CMOS**

  F.M. Wanlass et C.T. Sah

- **1964 – Premier MOS IC commercial**

  General Microelectronics

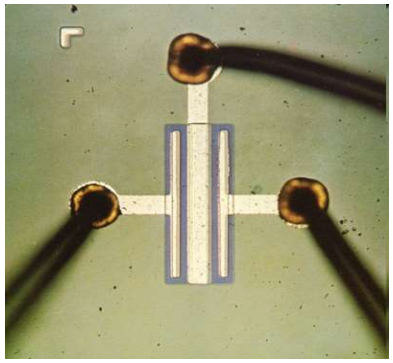
- **1971 – Premier microprocesseur**

  Intel i4004: 2300 transistors

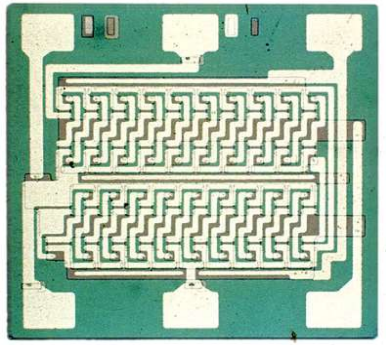
- **2007 – Intel Itanium 2**

  **> 1 milliard de transistors**

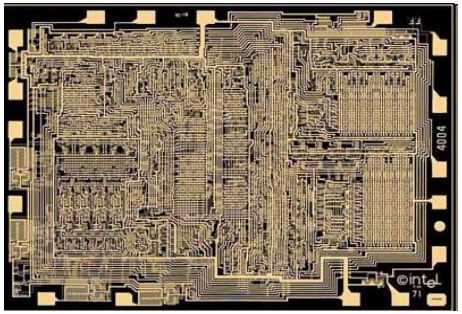
Fairchild FI 100
PMOS transistor



First commercial
MOS IC,
with **120 PMOS**



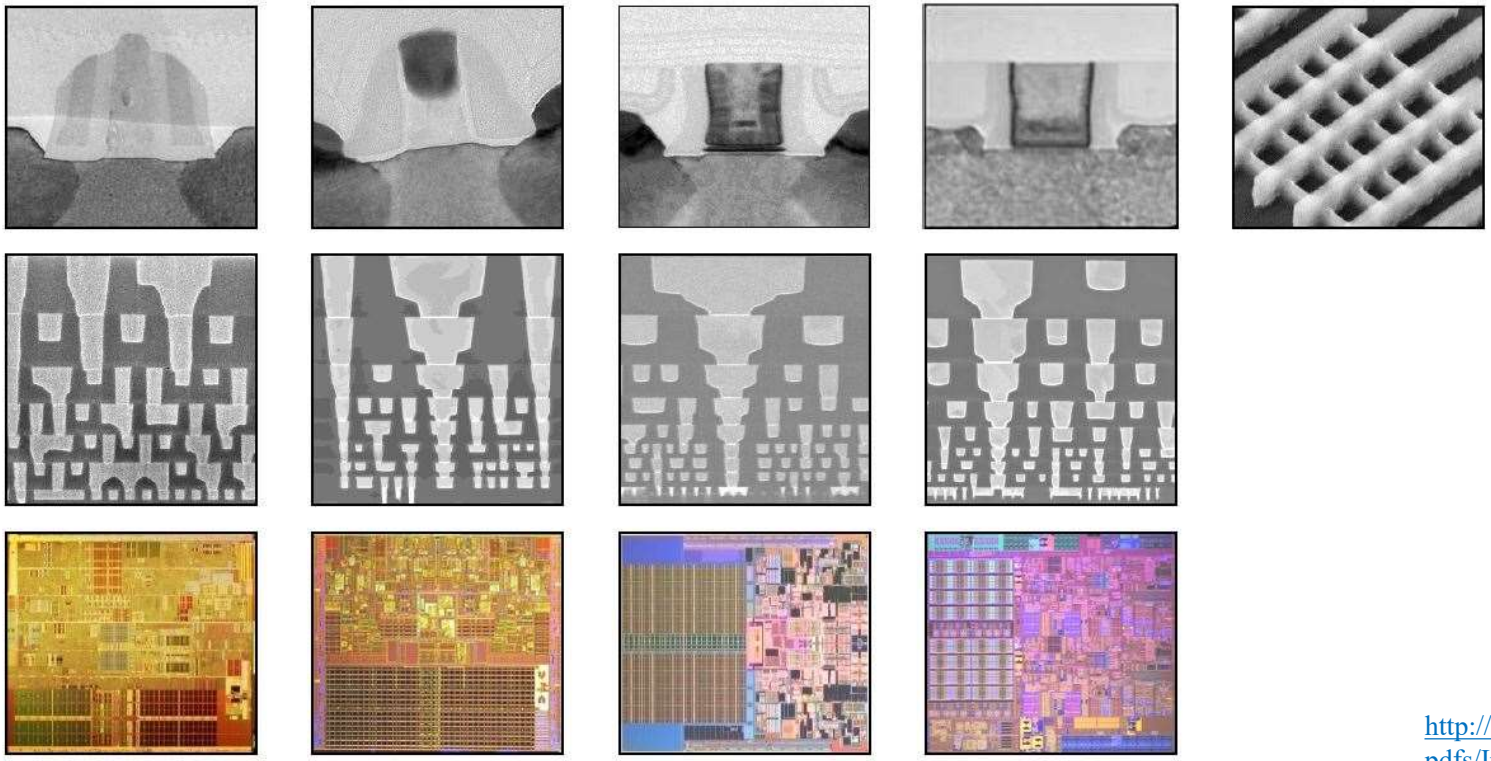
Intel i4004
with 2300 MOS

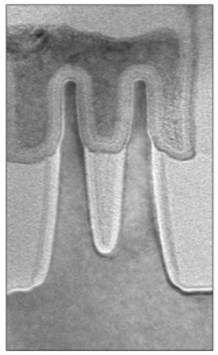


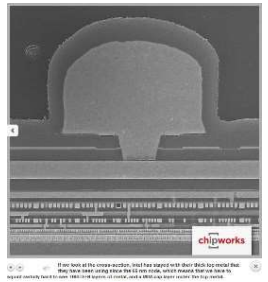
# VLSI (Very Large Scale Intgegration)

## FinFET by Intel

| 90 nm | 65 nm | 45 nm | 32 nm | 22 nm | **14 nm** | … |
|---|---|---|---|---|---|---|
| 2003 | 2005 | 2007 | 2009 | 2011 | 2014 | |







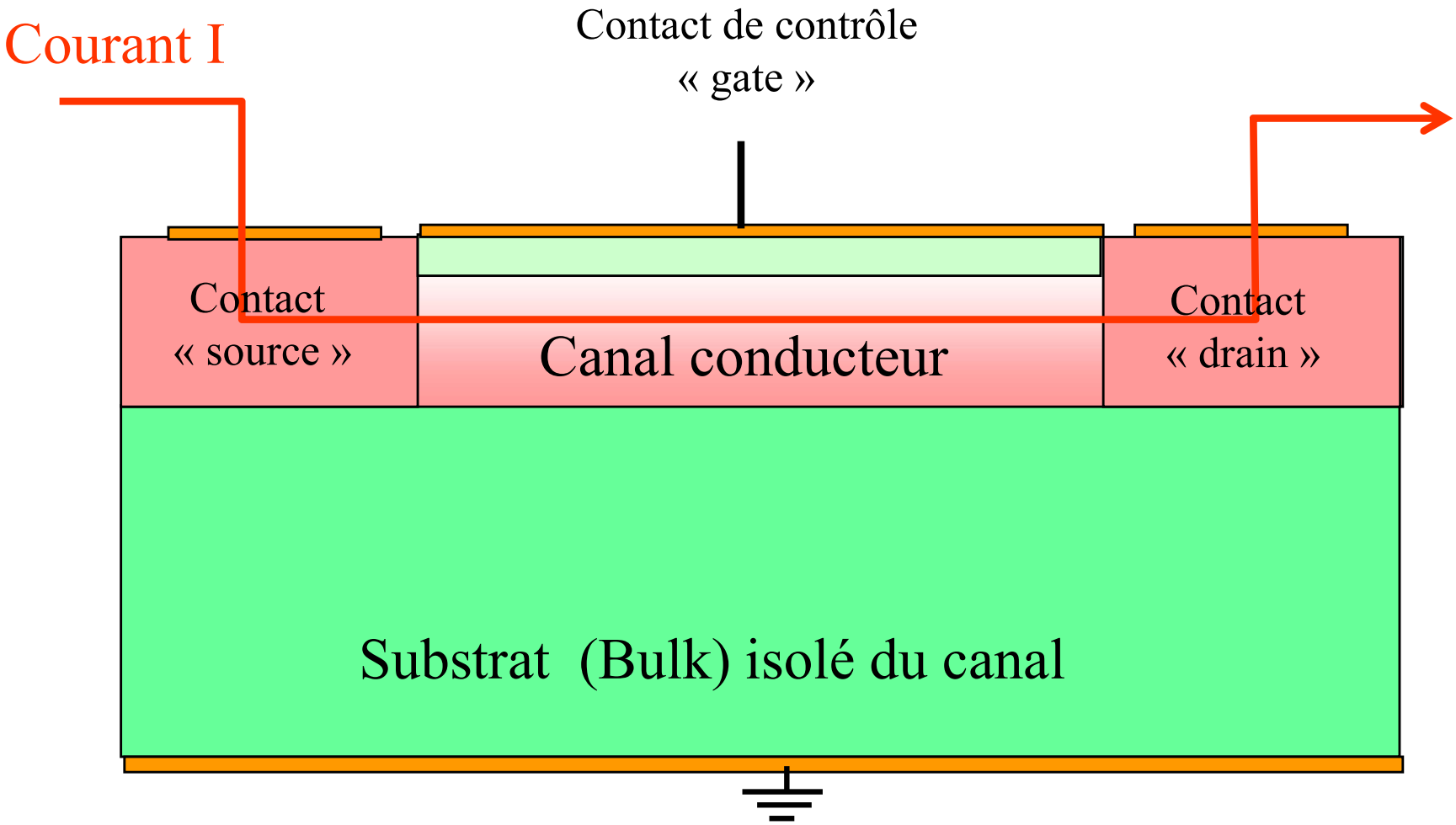
**13 metal layers**

M. Bohr «Intel's Revolutionary 22 nm Transistor Technology», INTEL May 2011

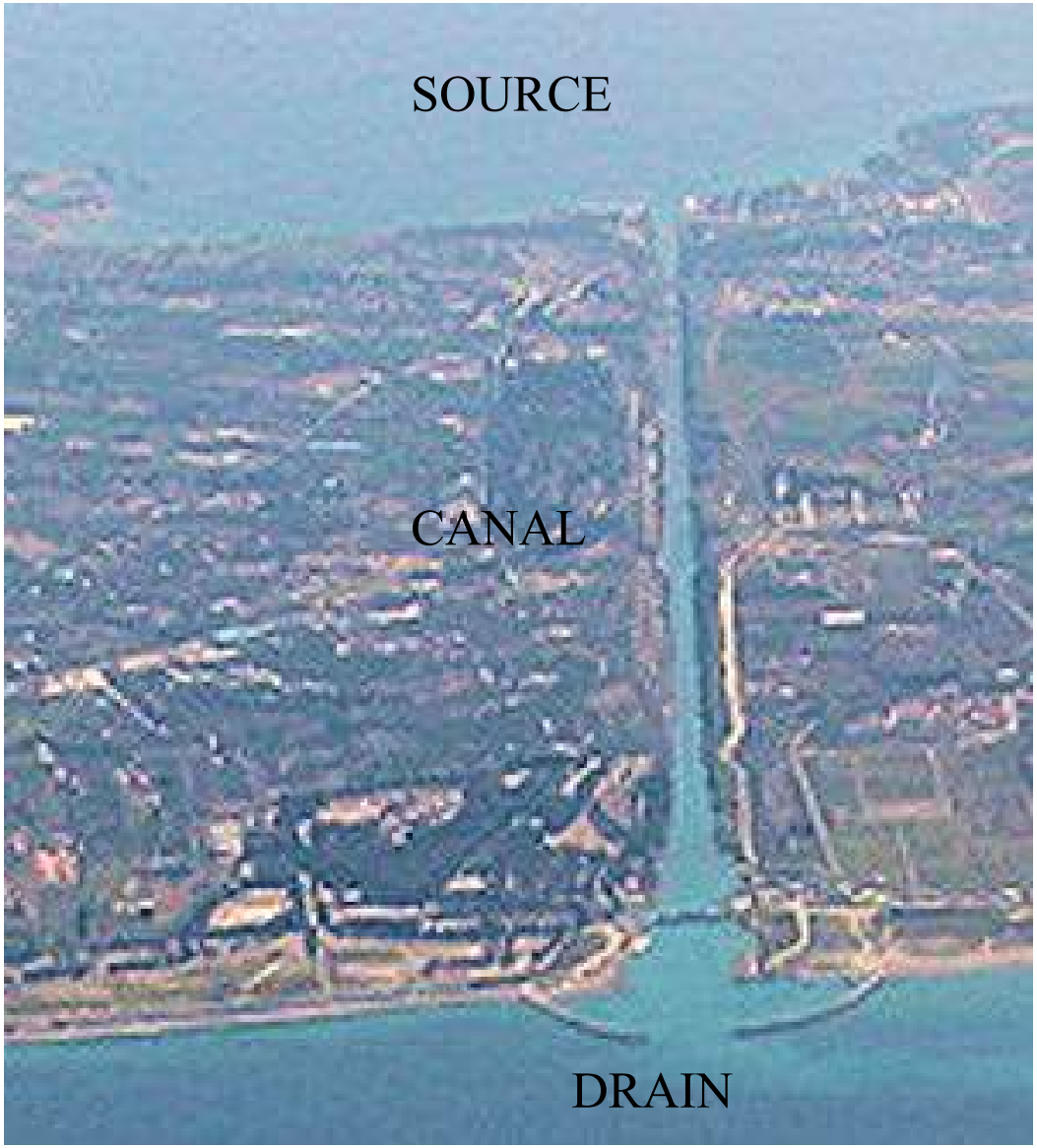
http://download.intel.com/newsroom/kits/14nm/pdfs/Intel_14nm_New_uArch.pdf

http://www.chipworks.com/en/technical-competitive-analysis/resources/blog/intels-14-nm-parts-are-finally-here/

# 10.1: Principe du Field Effect Transistor (FET)



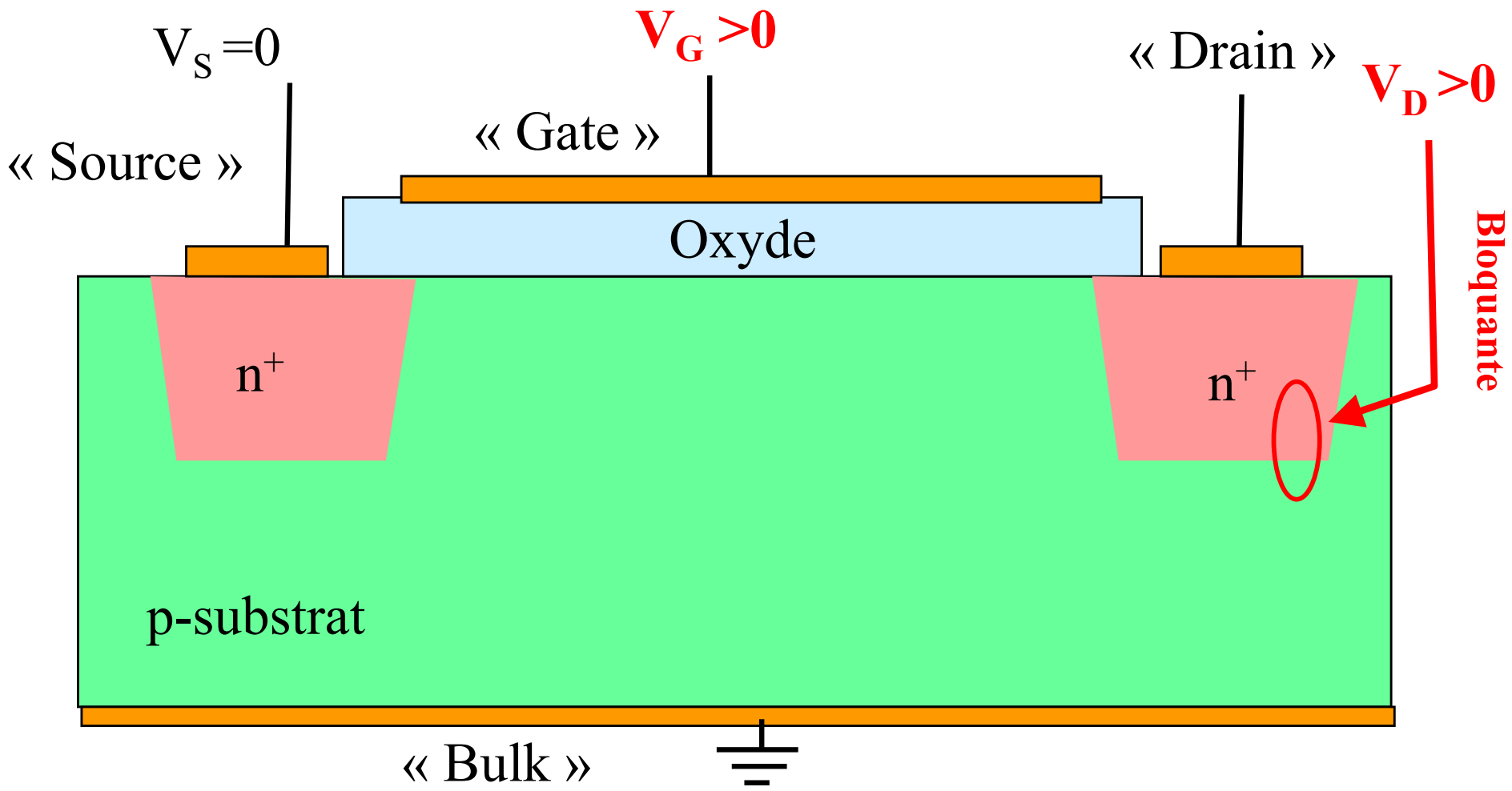
# Analogie: FET




Canal de Corinthe

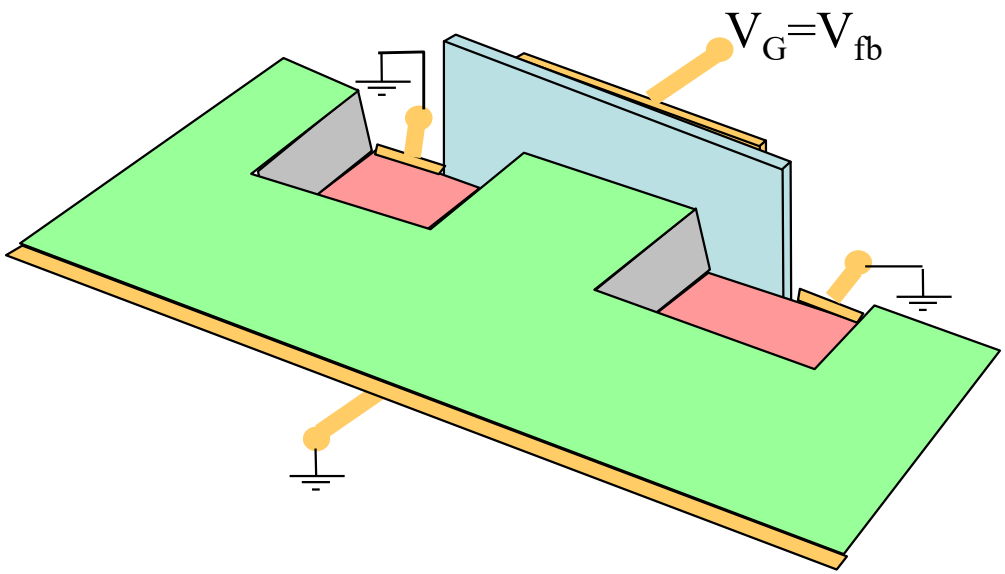
# Exemple 1: le NMOS

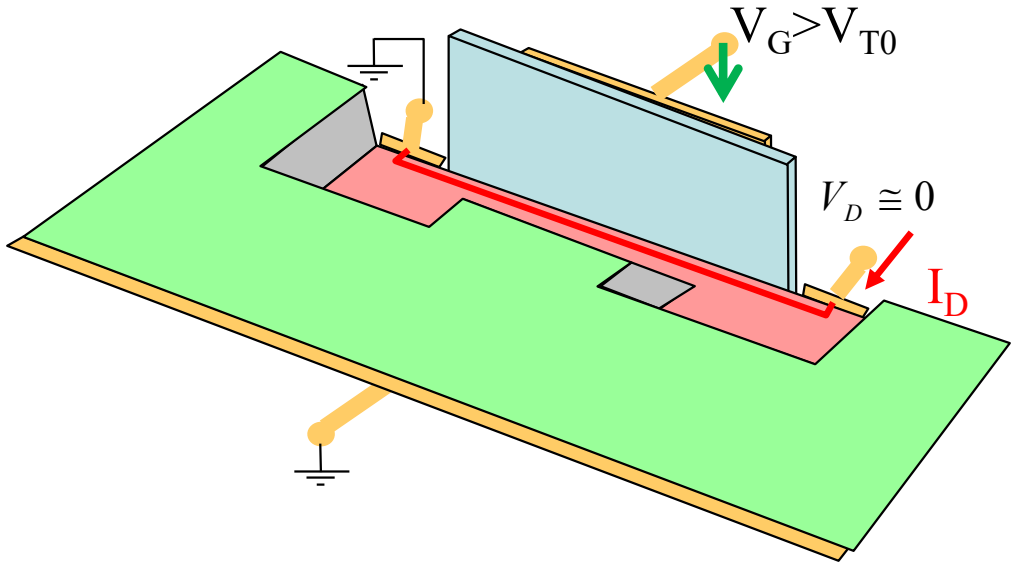
**Attirer des électrons dans le canal**



# Le NMOS, un “enhancement” FET

Bande de conduction



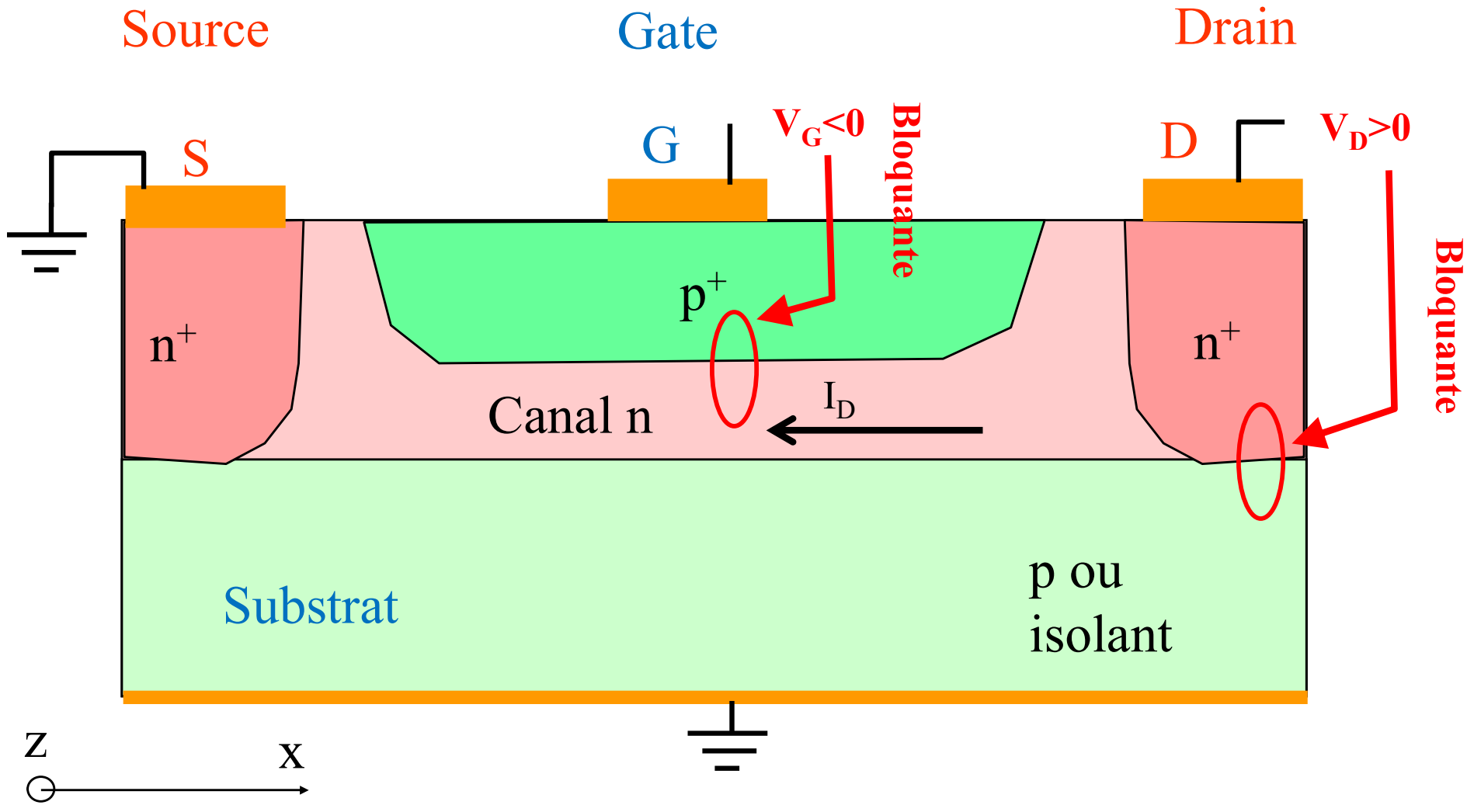

Sans tension de gate

Le canal n’existe pas

Avec tension de gate

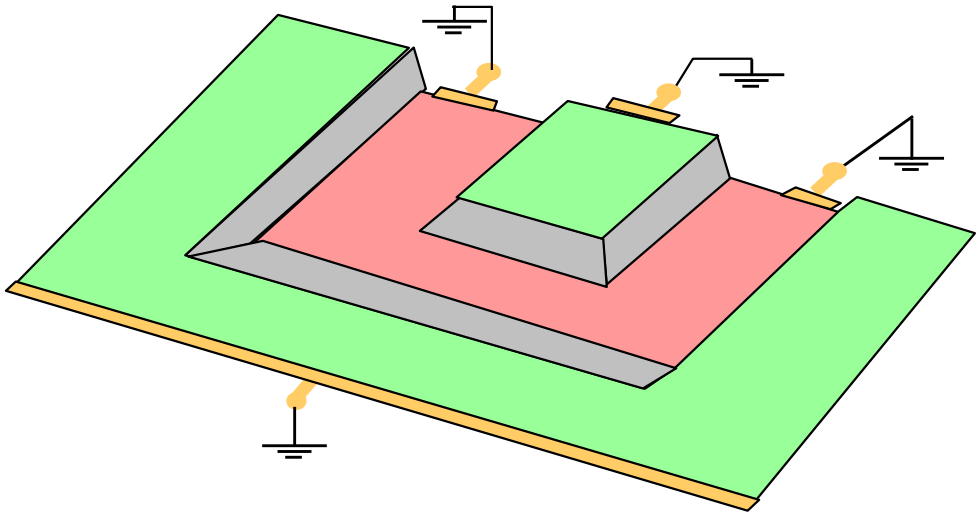
Le canal est créé

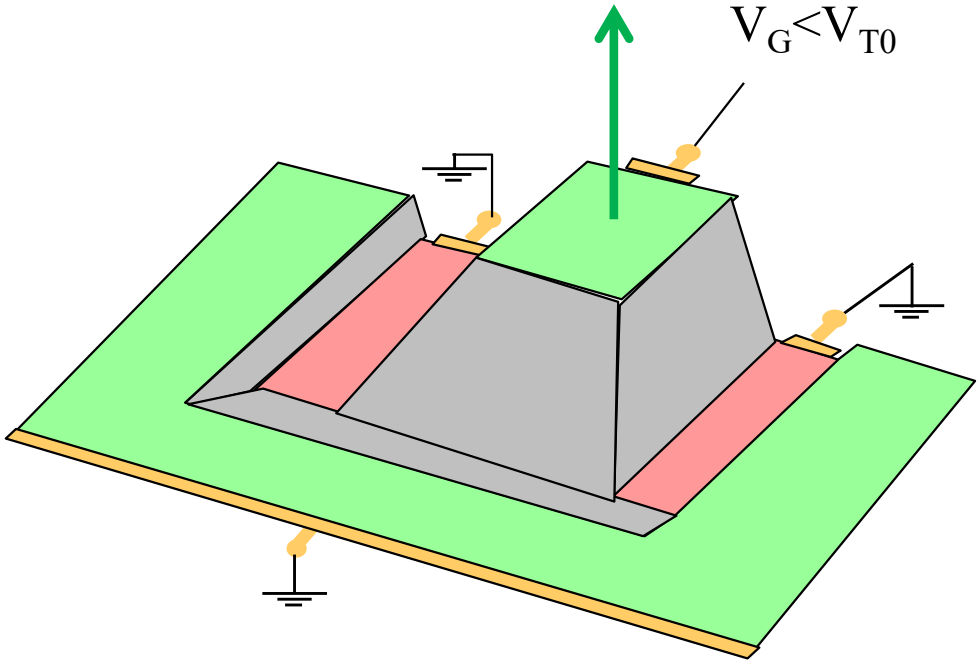
# Exemple 2: le JFET à canal n



# Le JFET à canal n: un « depletion » FET

Bande de conduction





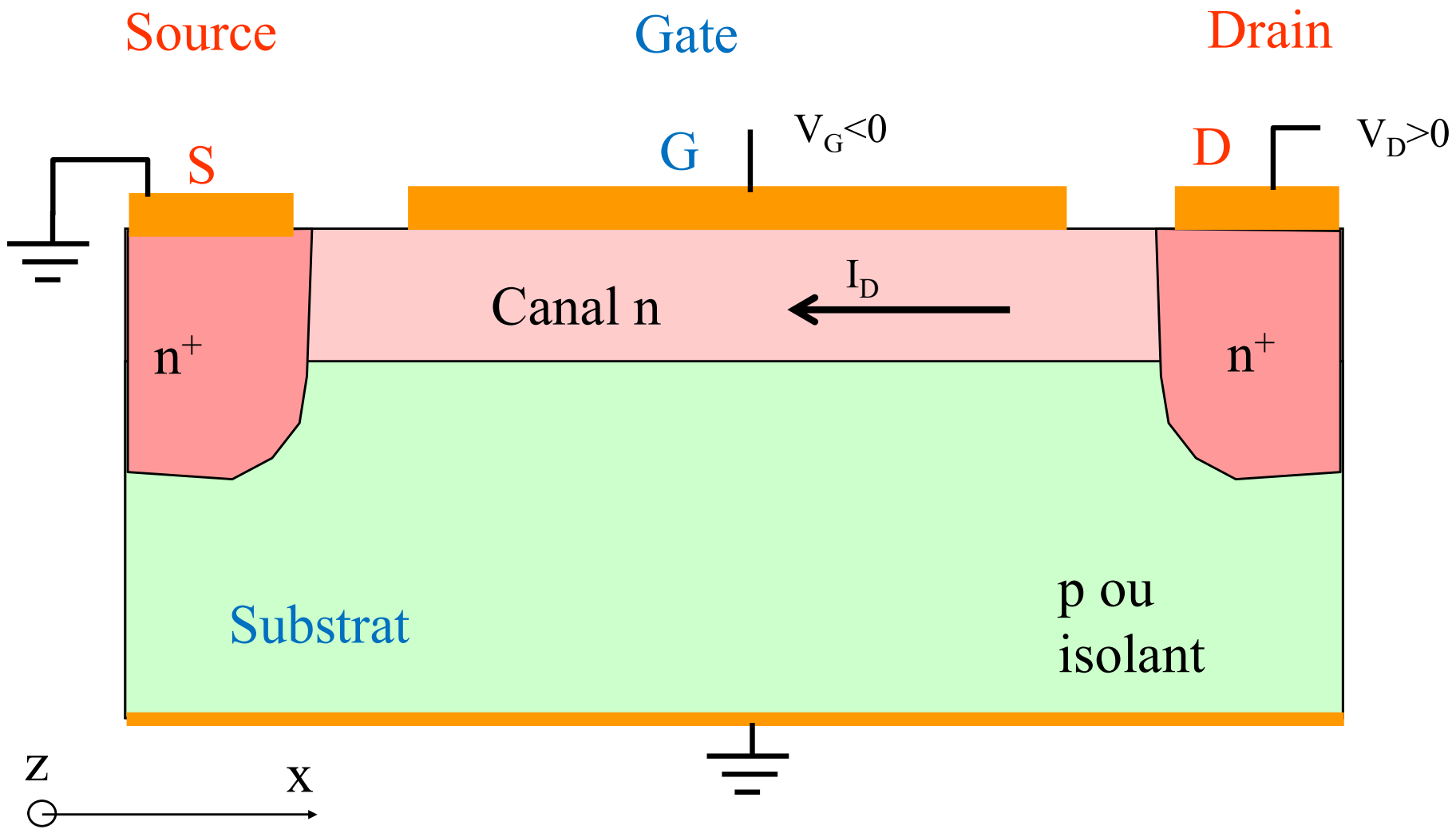

Sans tension de gate

Le canal existe

Avec tension de gate

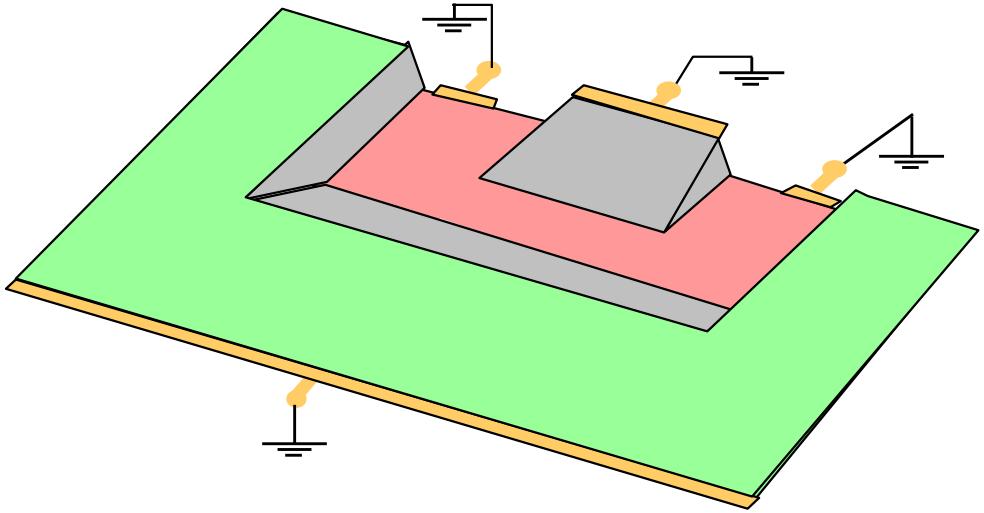
Le canal disparait

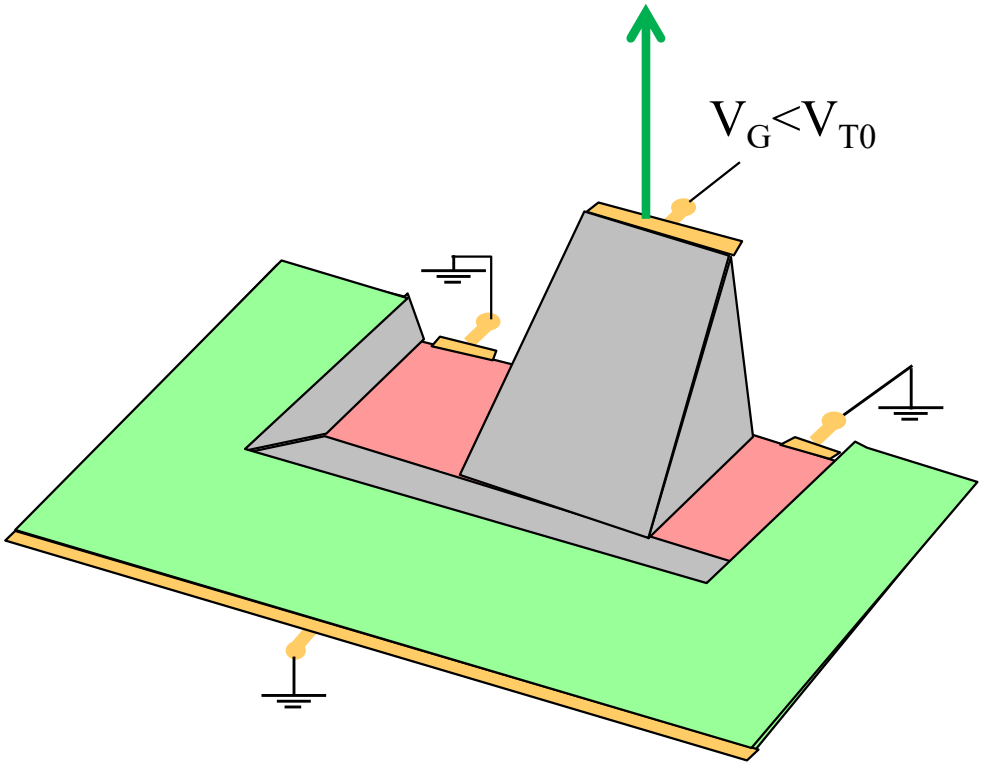
# MESFET à canal n



# MESFET à canal n

Bande de conduction





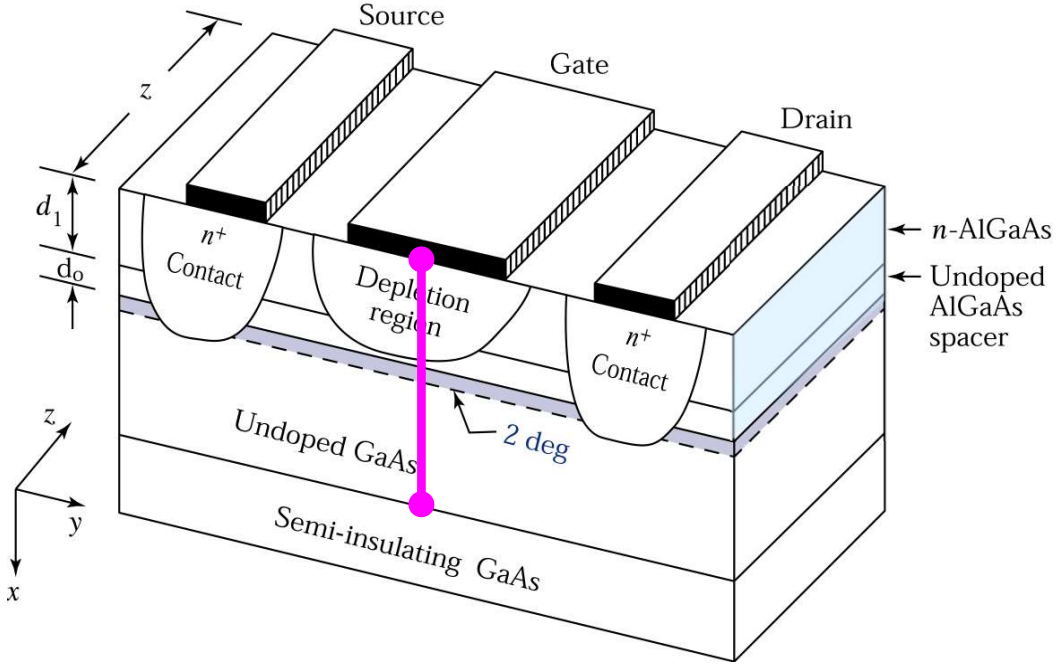

Sans tension de gate

Le canal existe

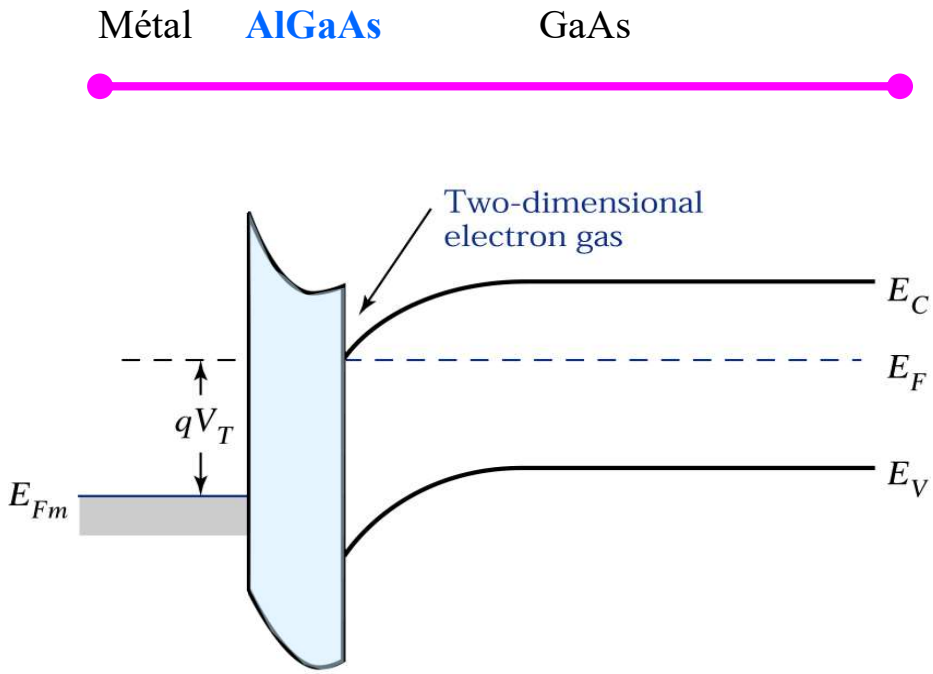
Avec tension de gate

Le canal disparait

# High Electron Mobility Transistors (HEMT)

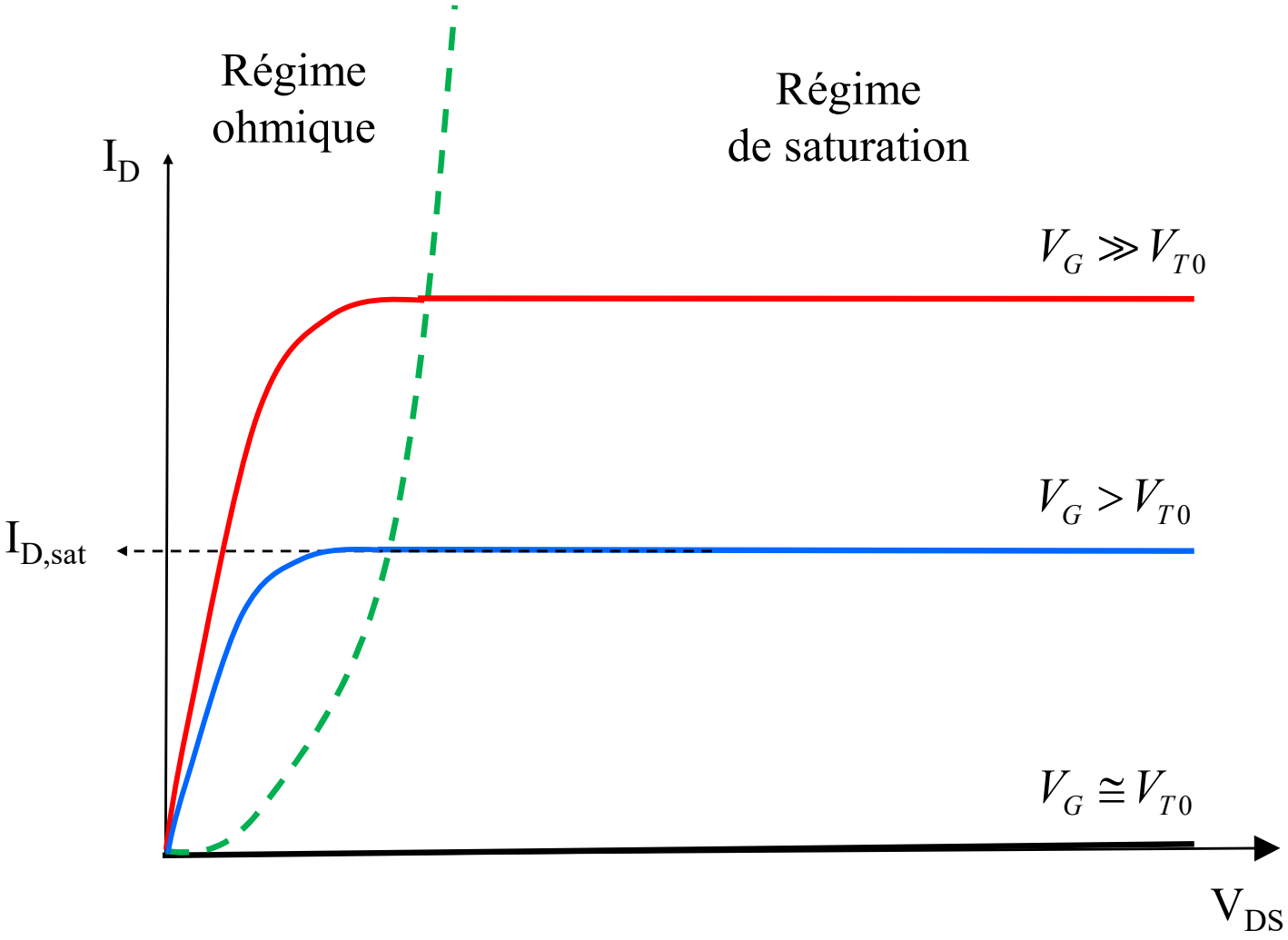



*Semiconductor Devices, 2/E* by S. M. Sze




*Semiconductor Devices, 2/E* by S. M. Sze

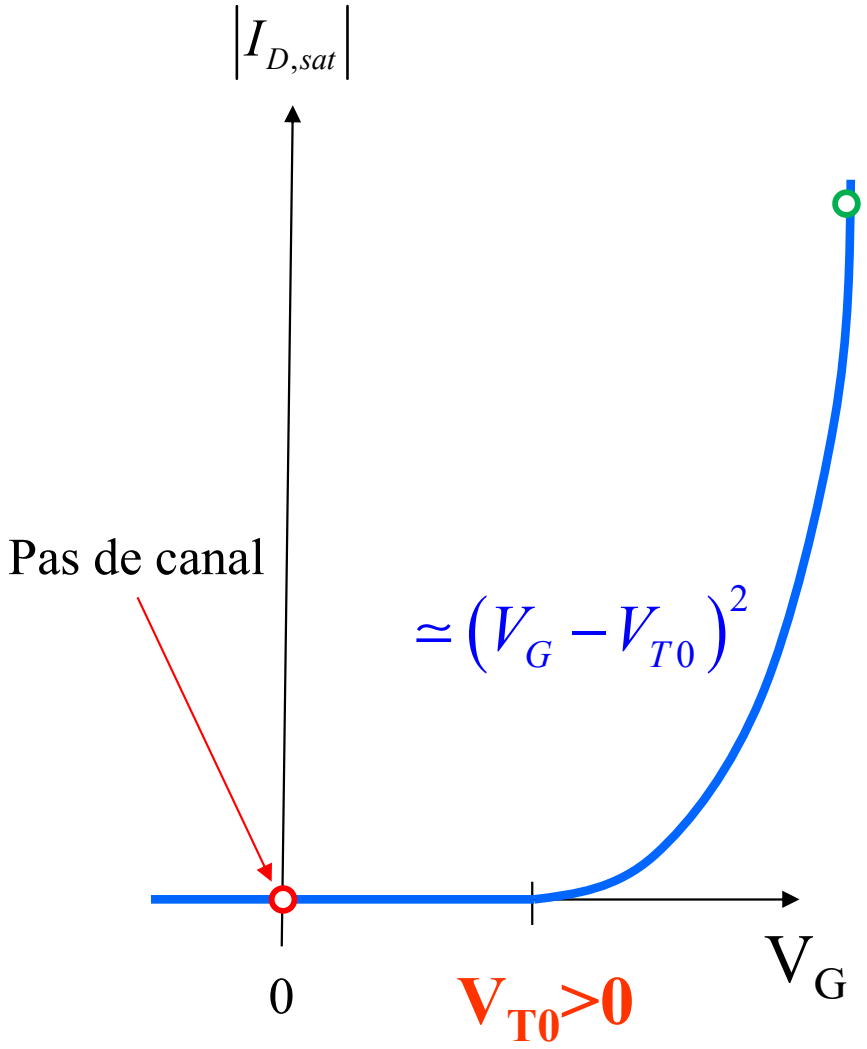
# Courbes de sortie des FET idéaux (canal n)



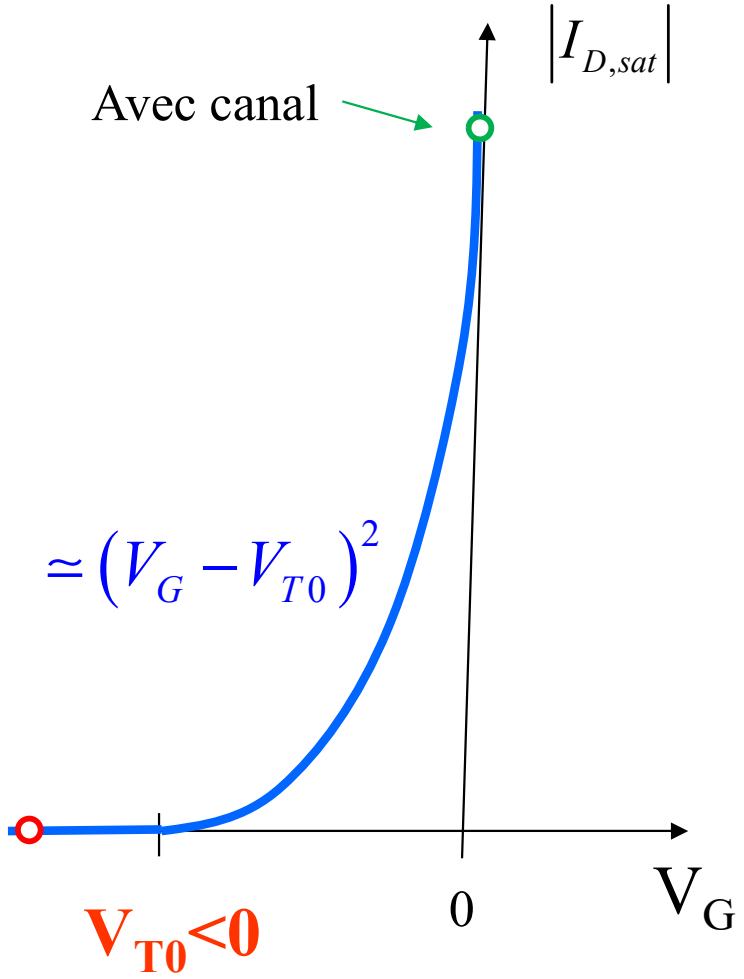

| | **NMOS** | **N-JFET** |
|---|---|---|
| $V_G \gg V_{T0}$ | $V_G \gg 0$ | $V_G = 0$ |
| $V_G > V_{T0}$ | $V_G > 0$ | $V_G < 0$ |
| $V_G \cong V_{T0}$ | $V_G = 0$ | $V_G << 0$ |
| | $V_{T0} > 0$ | $V_{T0} < 0$ |

# Tension de threshold et courbe $I_{D,sat}(V_G)$

## NMOS

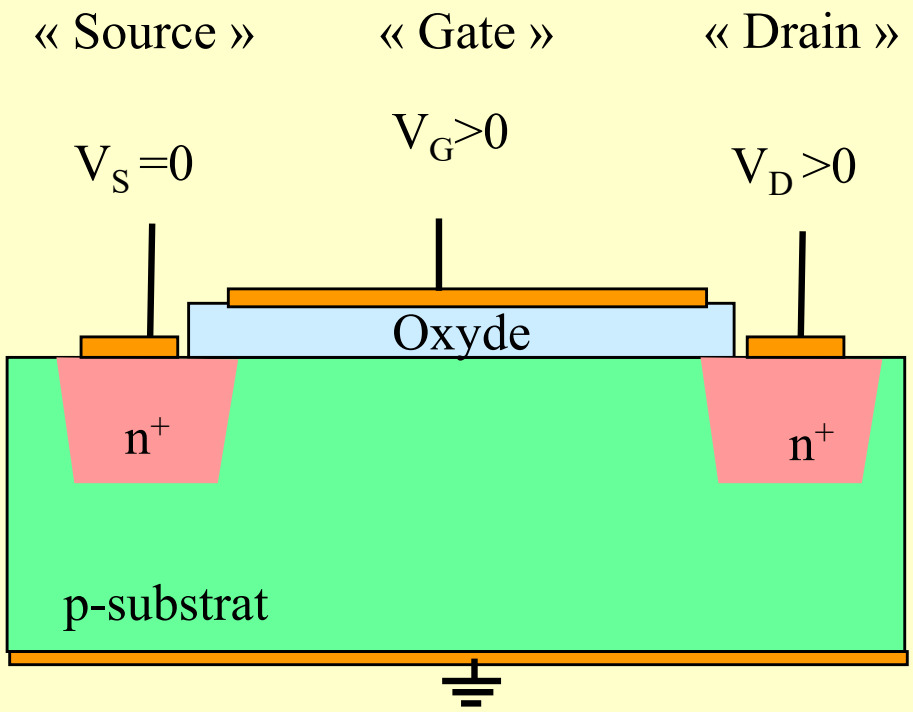



## JFET à canal N

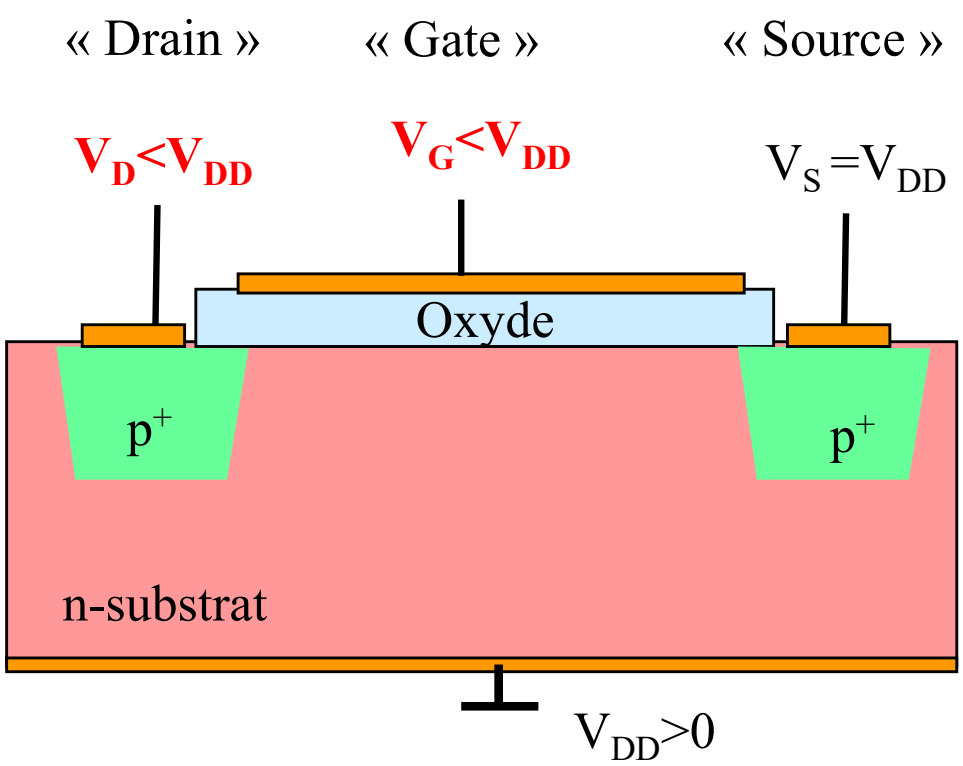


# 10.2: Structure MOSFET

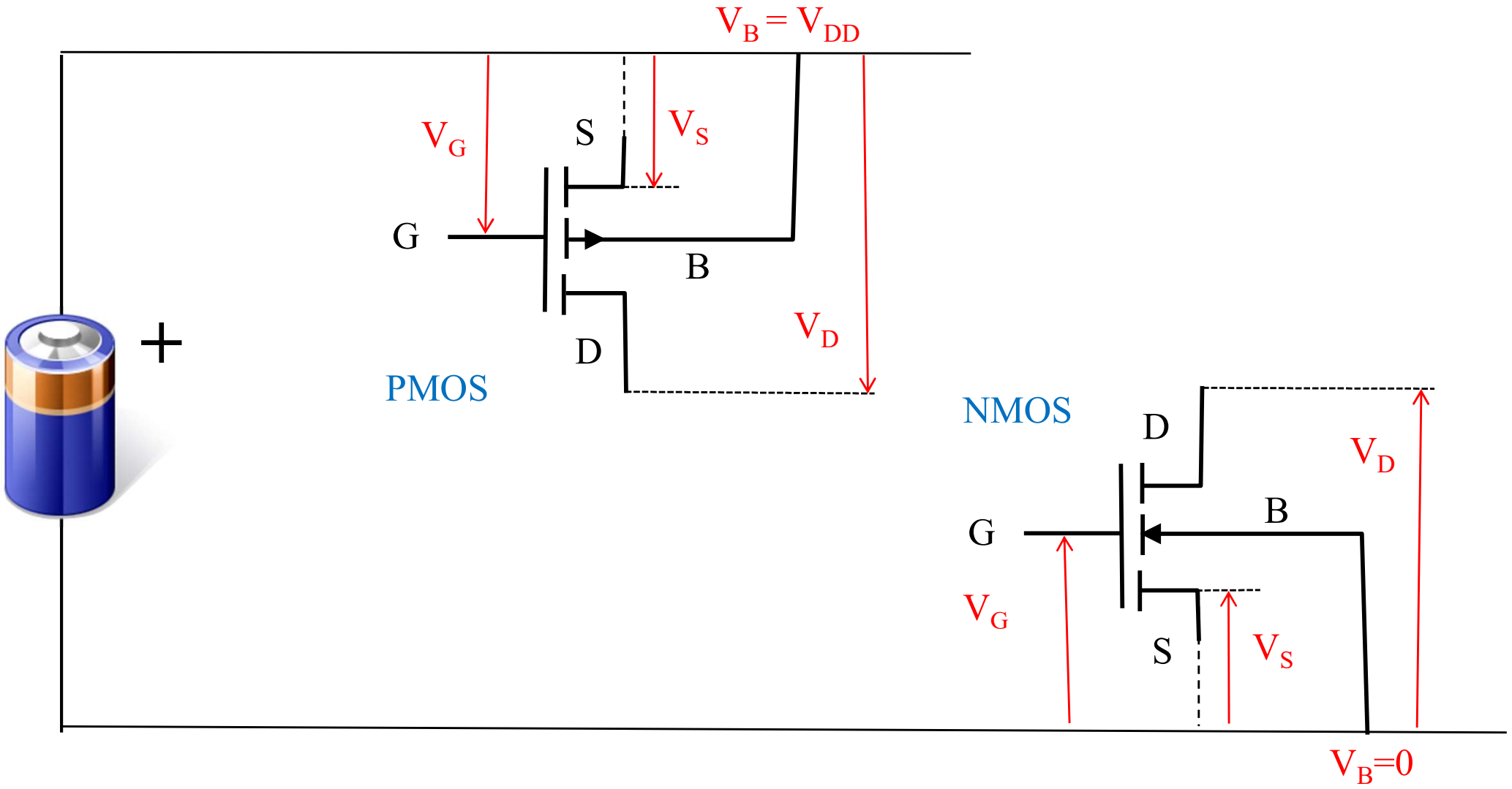
NMOS: MOSFET à canal n



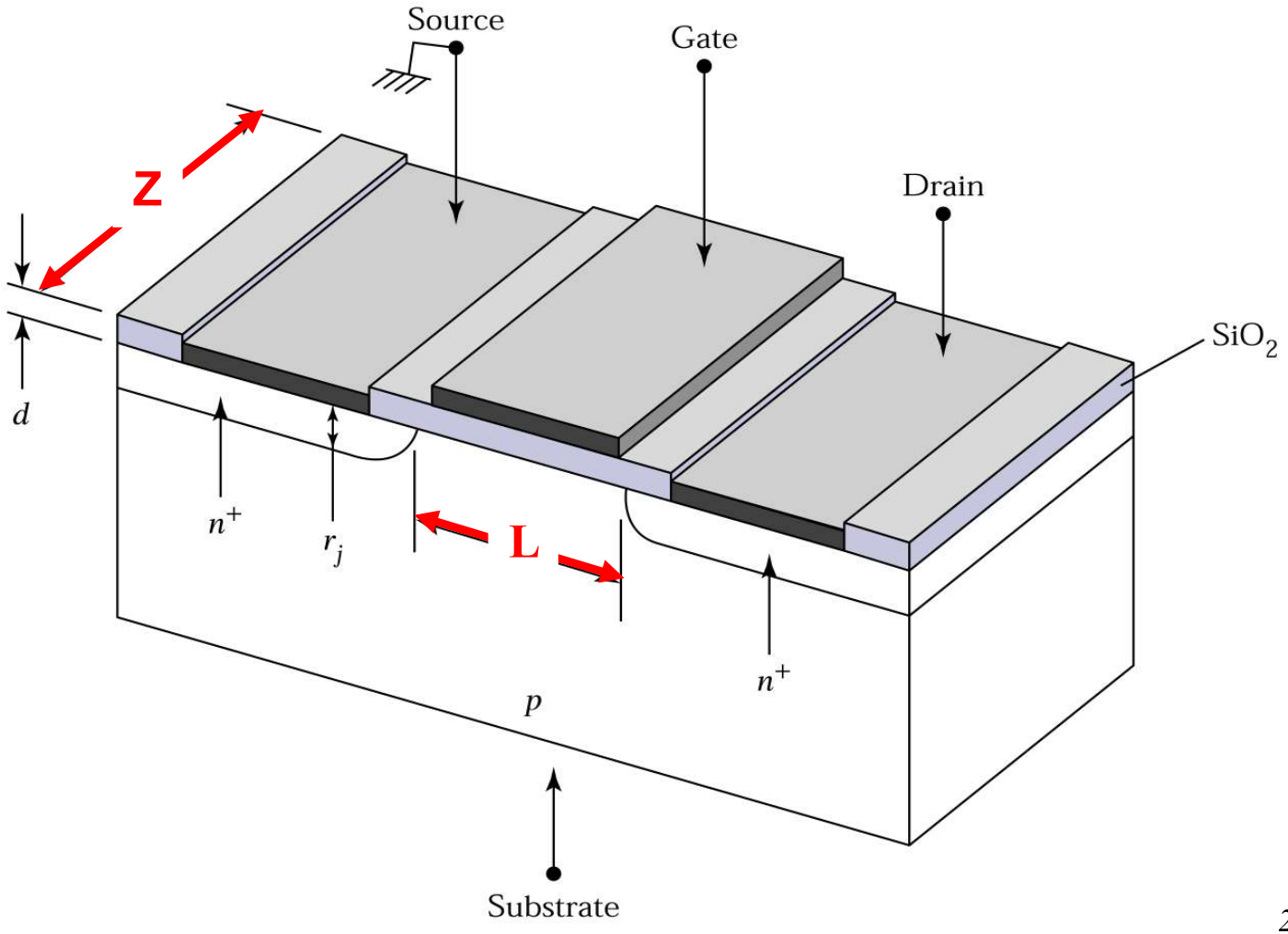

PMOS: MOSFET à canal p



# MOSFET: définition des tensions



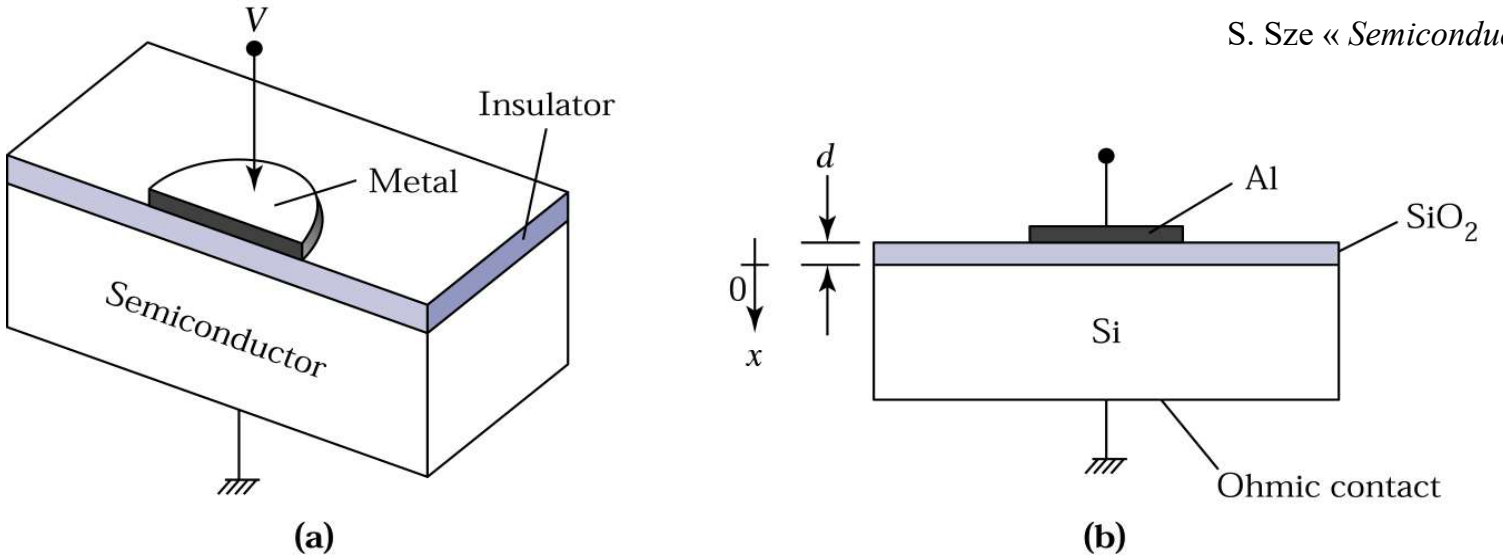
# NMOS




*2/E* by S. M. Sze

# Rappel: structure MOS

S. Sze « *Semiconductor devices* »




**"Metal"**

Al, Au,
(electromigration)

Poly-Si, Silicide

**Oxide**

$SiO_2$, High k (HfSiON)

$d_{ox} \cong 10\,nm$

$C_{ox} = \varepsilon_r \varepsilon_0 \frac{A}{d_{ox}}$

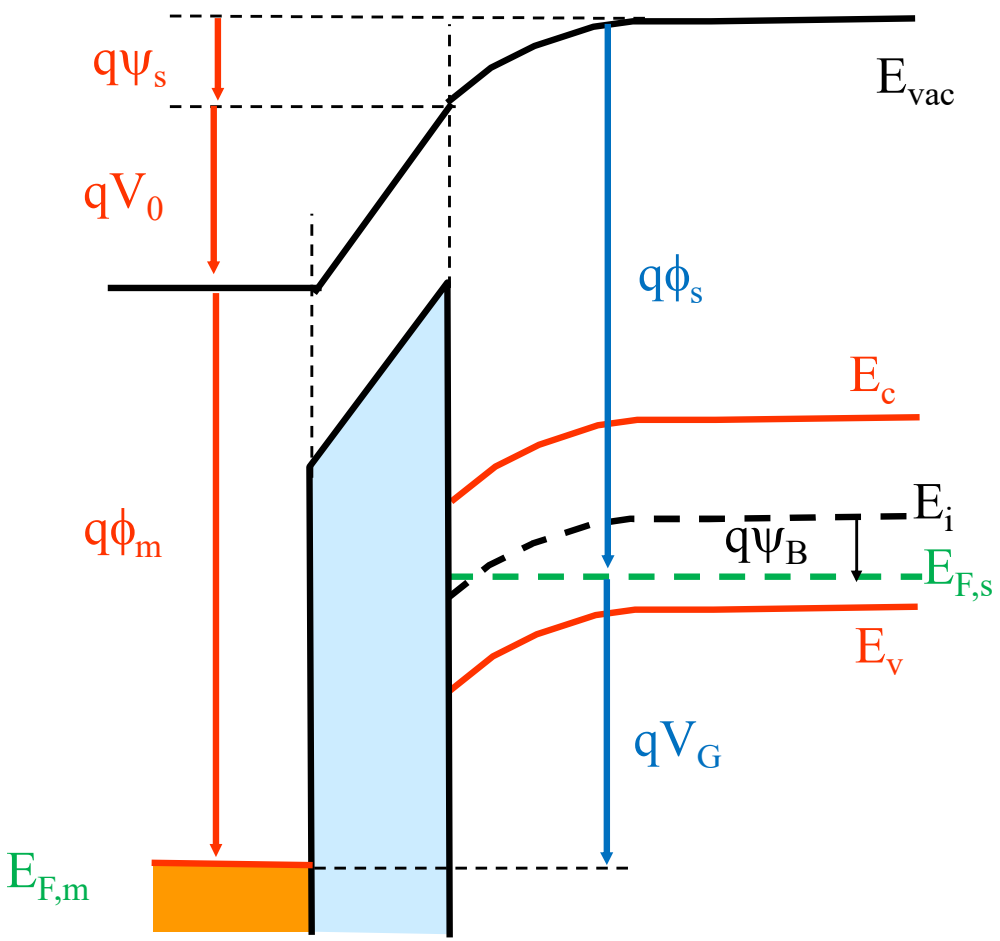
$\varepsilon_r \cong 4 \quad (SiO_2)$

**Semiconductor**

Silicon

$N \approx 10^{16}\,cm^{-3} \rightarrow 10^{18}\,cm^{-3}$

# Rappel: Potentiels et tensions




Potentiel sur le métal $V_G$:

$$V_G + \phi_s = \psi_s + V_0 + \phi_m$$

$$V_{M0} - V_{fb} = 2\psi_B \cdot (2n - 1)$$

$$V_G - V_{M0} \cong n \cdot (\psi_s - 2\psi_B) - \frac{Q_n}{C_{ox}}$$

# Rappel: Inconnues et équations pour une jonction MOS sur substrat p

## 2 inconnues

A) Potentiel de surface $\psi_s$ :

$$\psi_s$$

B) Charge libre à l'interface $Q_n$ reliée au potentiel sur l'oxyde

$$Q_n$$

## Threshold

$$V_{M0} - V_{fb} = 2\psi_B \cdot (2n - 1)$$

## 2 équations en fct de $V_G$:

1) $$V_G - V_{M0} \cong n \cdot (\psi_s - 2\psi_B) - \frac{Q_n}{C_{ox}}$$

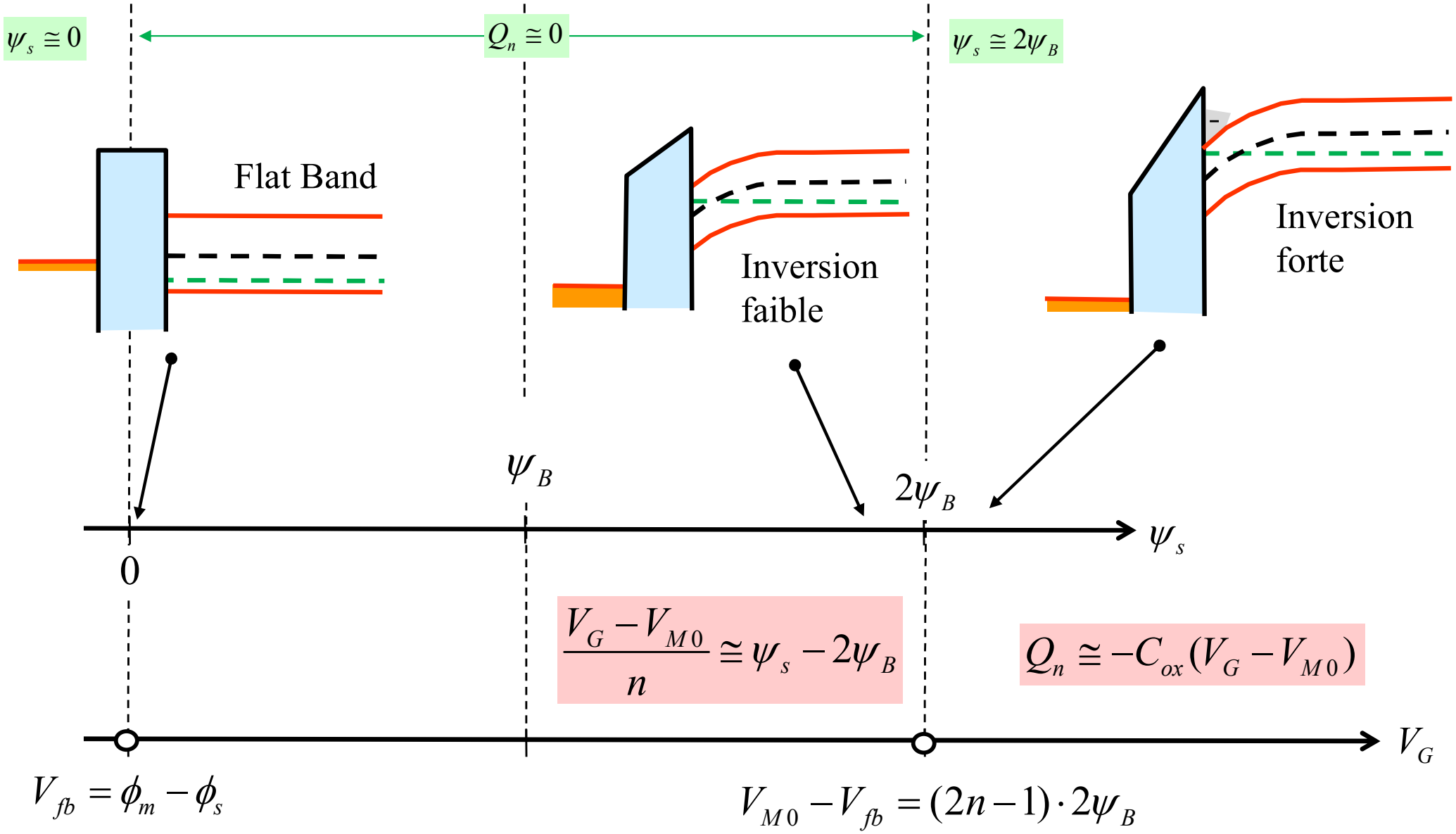
2) Approximations

- Accumulation $\psi_s \cong 0$

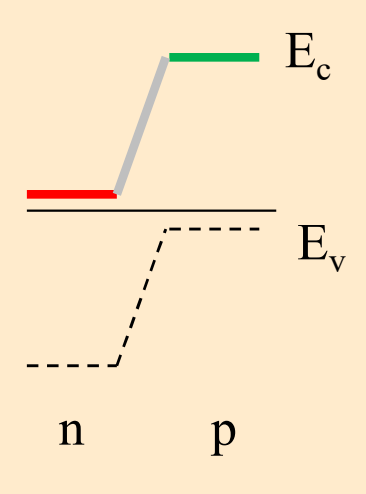
- Déplétion
- **Inversion faible** $Q_n = 0$
- Déplétion profonde

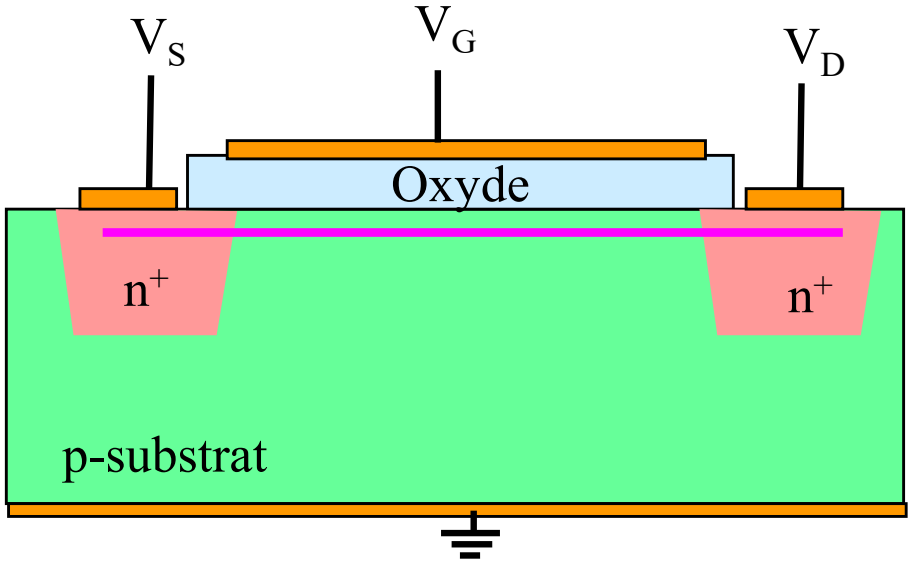
- **Inversion forte** $\psi_s \cong 2\psi_B$

# Résumé: Formules avec slope factor n



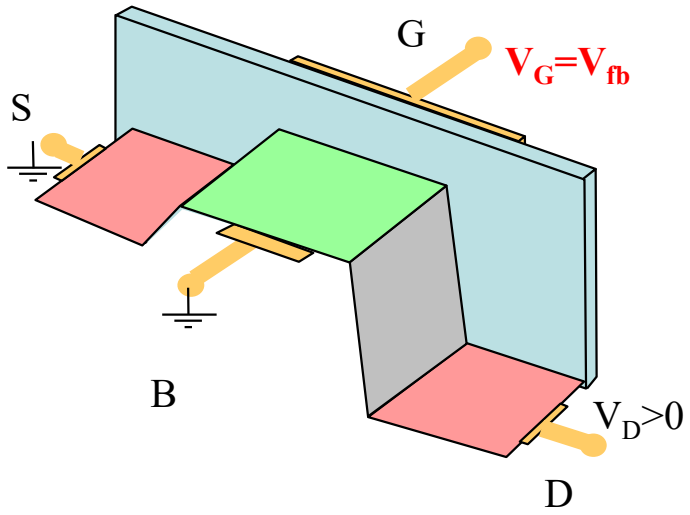
# 10.3: Fonctionnement « sub-threshold »



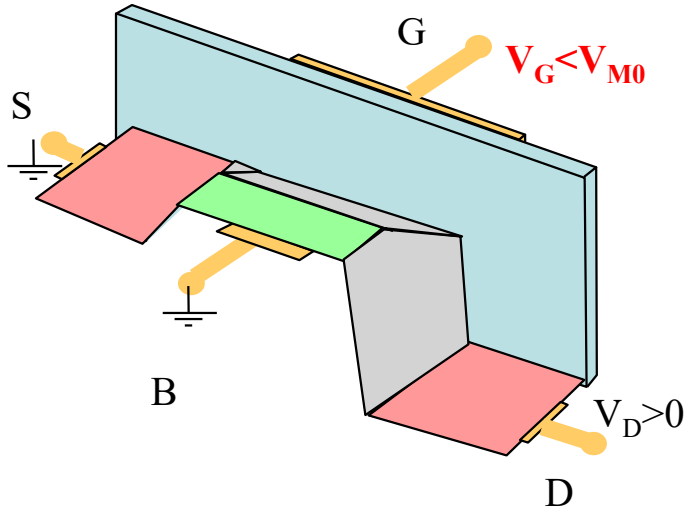




→ **Structure npn**

**Flat-band**

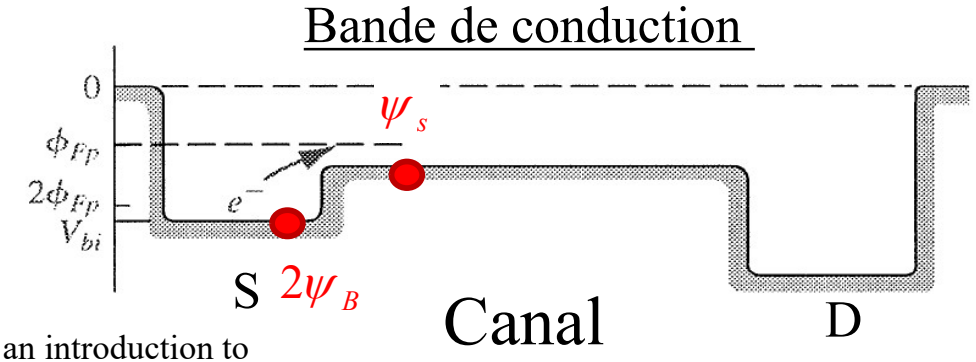



**Inversion faible**

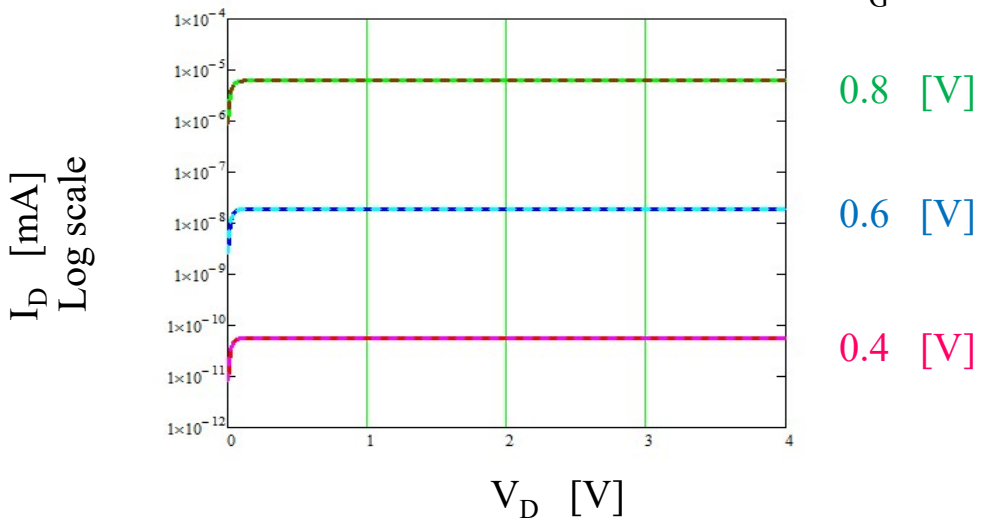


# Fonctionnement « sub-threshold »: inversion faible

- Comportement similaire à un transistor bipolaire npn
- Pas de champ électrique → courant de diffusion




Neamen, « an introduction to semiconductor devices »

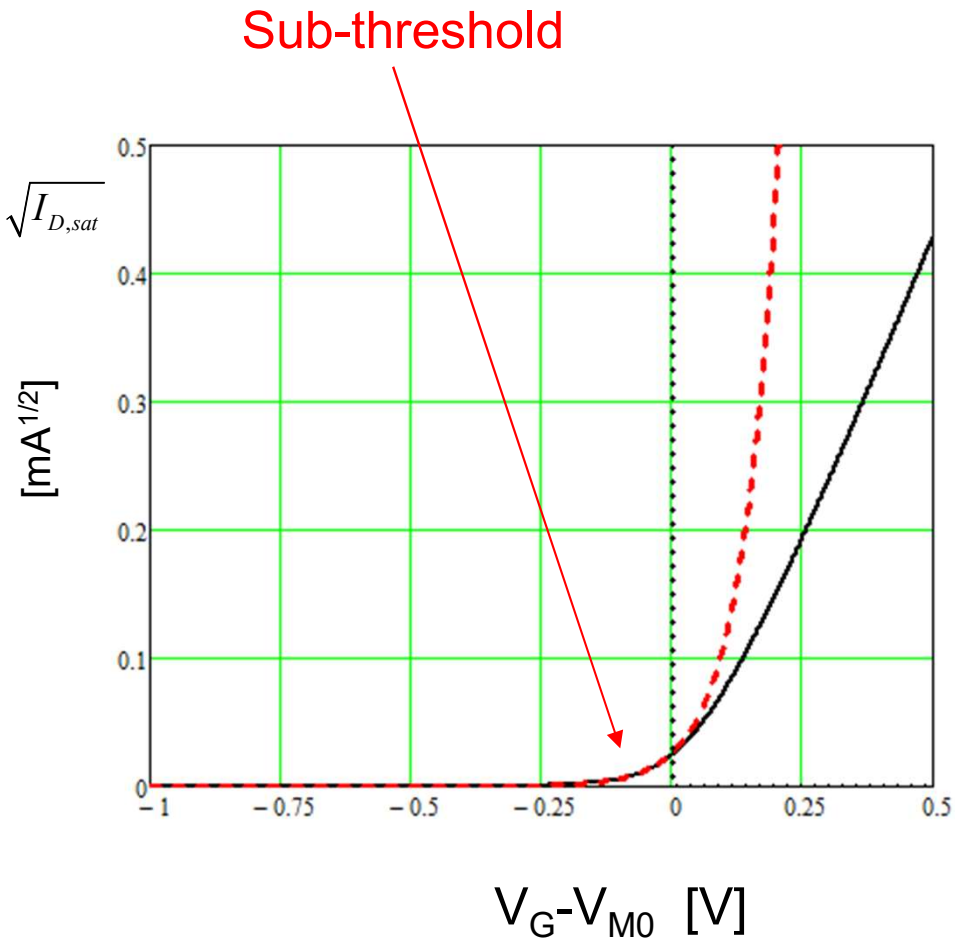


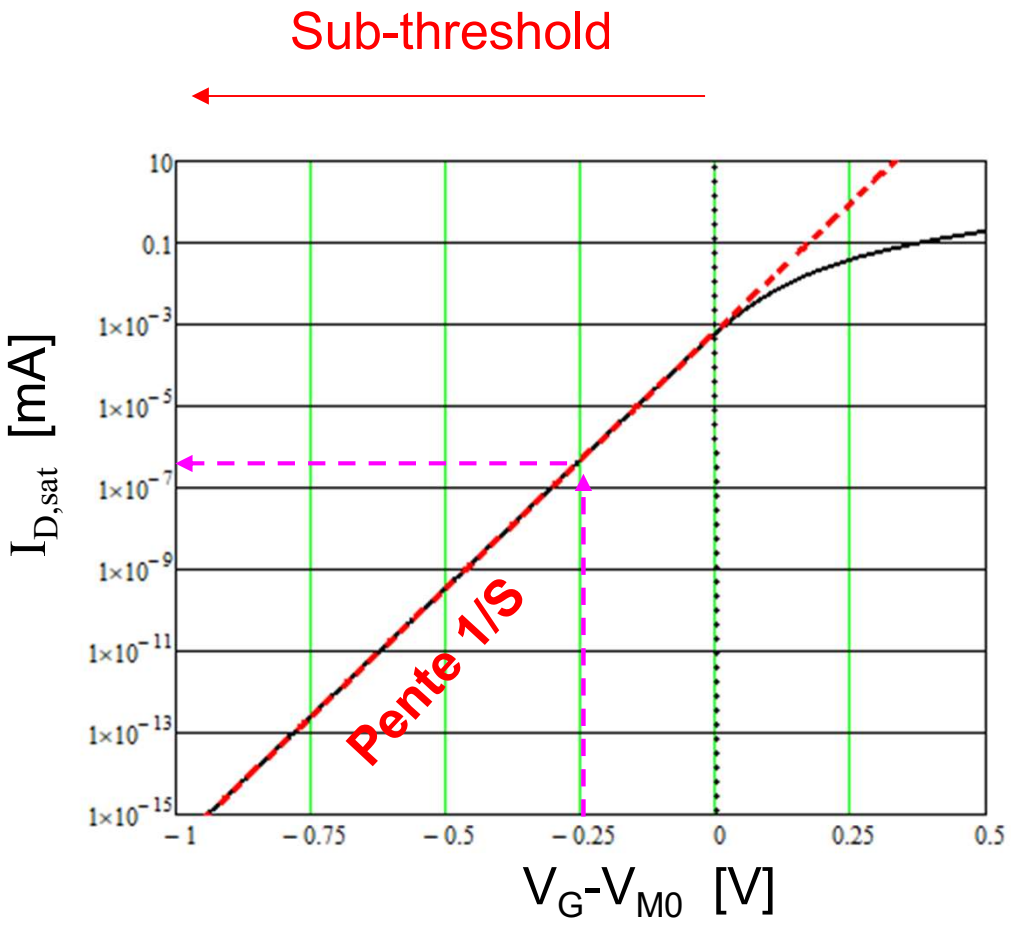

$$\frac{V_G - V_{M0}}{n} \cong (\psi_s - 2\psi_B) - \frac{Q_n}{nC_{ox}}$$

$$I_{D,sat} \approx I_{sub,0} \cdot e^{\frac{(V_G - V_{M0})}{n} \cdot \frac{1}{U_T}}$$

$$\frac{g_{m,sat}}{I_{D,sat}} \equiv \frac{1}{I_{D,sat}} \cdot \frac{\partial I_{D,sat}}{\partial V_G} \approx \frac{1}{n \cdot U_T}$$

# Opération « sub-threshold »: exemple en mode actif ($V_D > V_{D,sat}$)



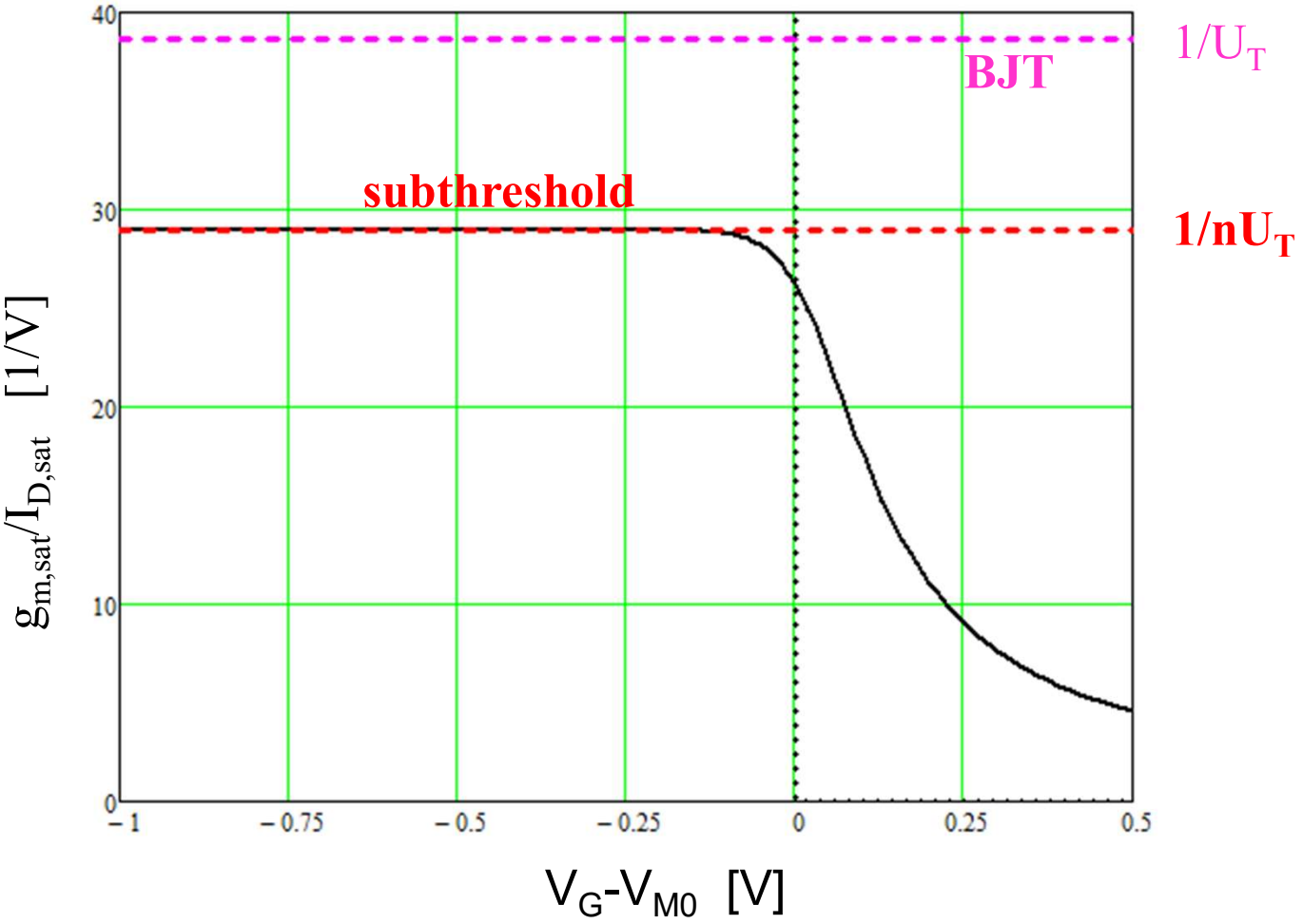

$C_{ox}$=3fF/um$^2$
W/L=10
T=300 K

$u_n$=1000cm$^2$/V.s
n=4/3

$$S = n \cdot U_T \cdot Ln(10)$$

300K → S=n.60 mV/dec.

# Transconductance en saturation: $g_m/I_D$




Transconductance définition

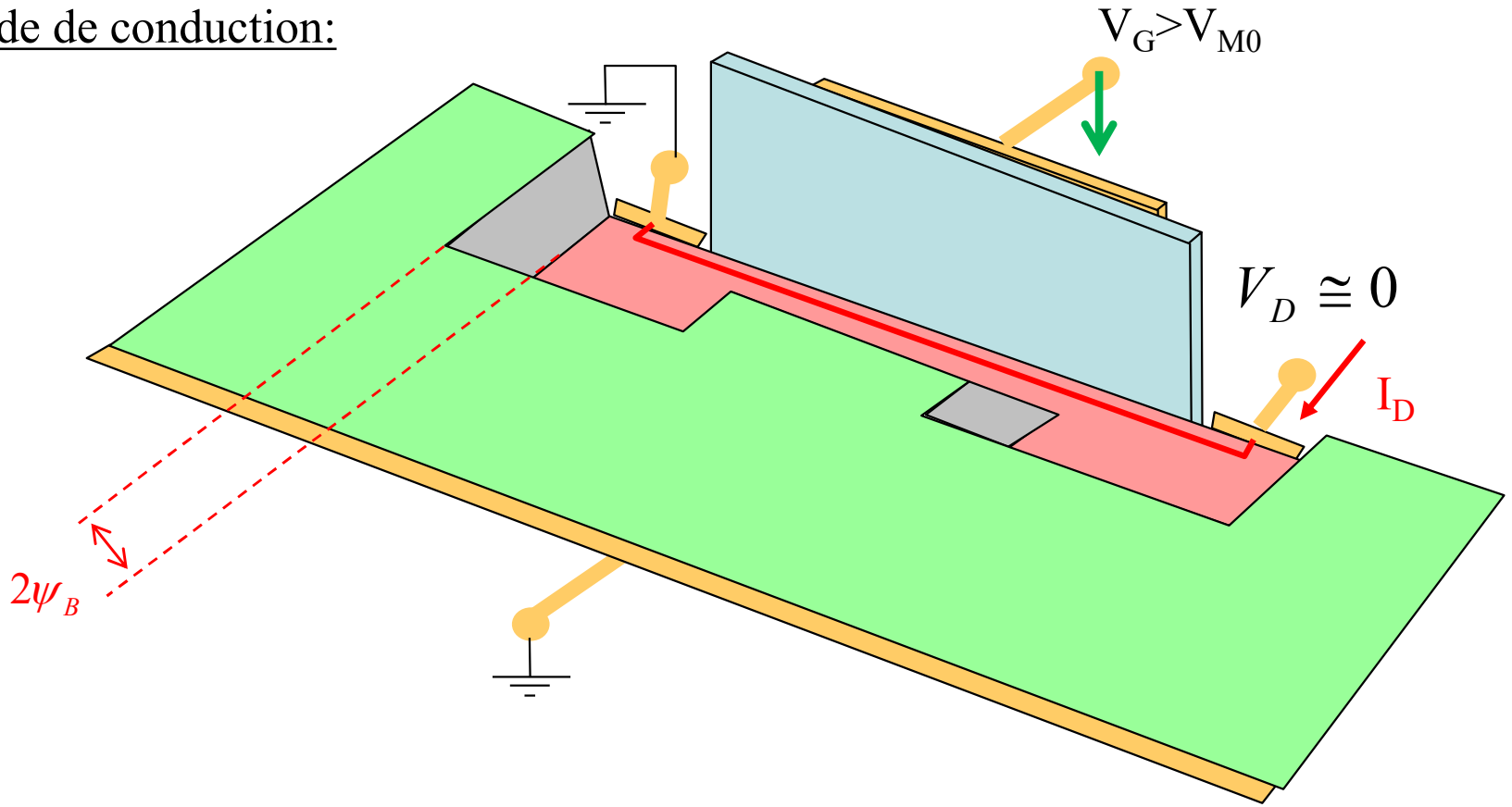
$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G}$$

$C_{ox}$=3fF/um$^2$
W/L=10
T=300 K

$u_n$=1000cm$^2$/V.s
n=4/3

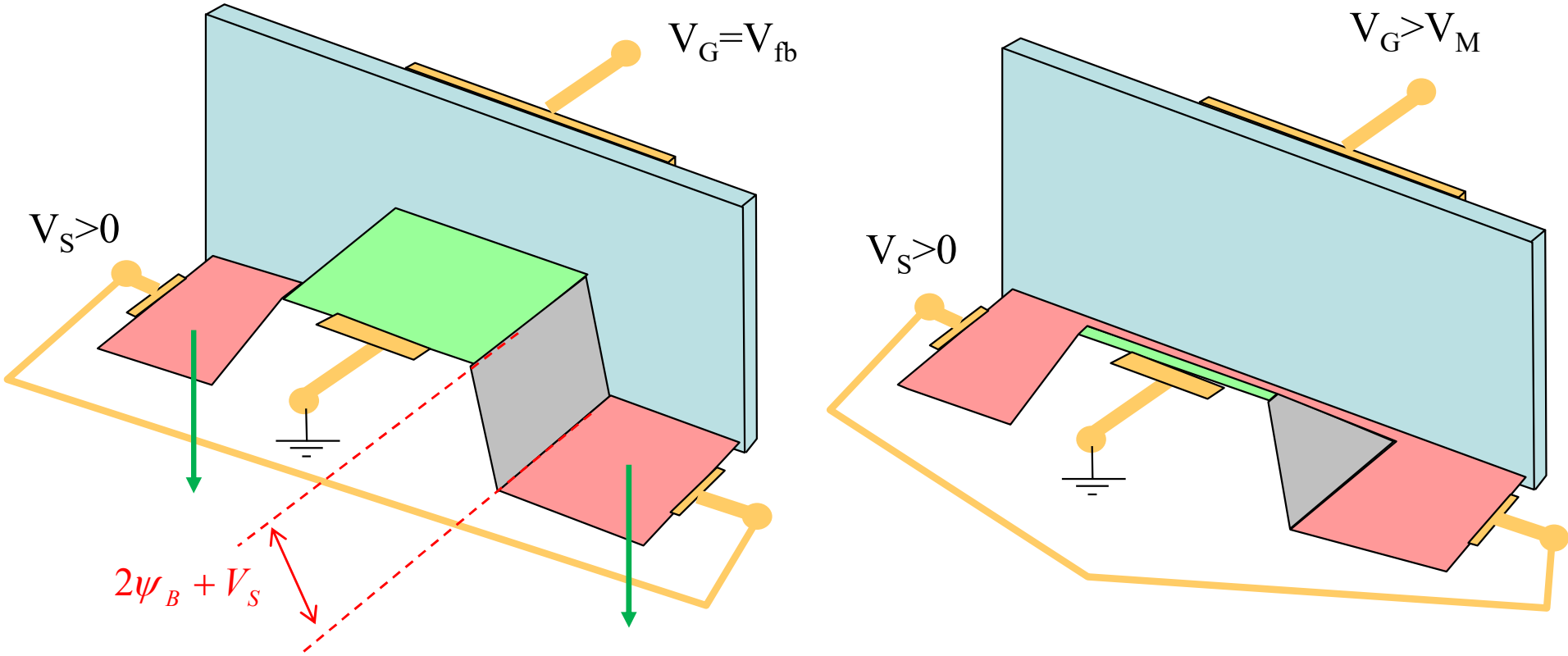
# 10.4: NMOS en inversion forte, régime linéaire

Bande de conduction:




$$|Q_n| = C_{ox}\,(V_G - V_{M0})$$

# Influence de $V_S$



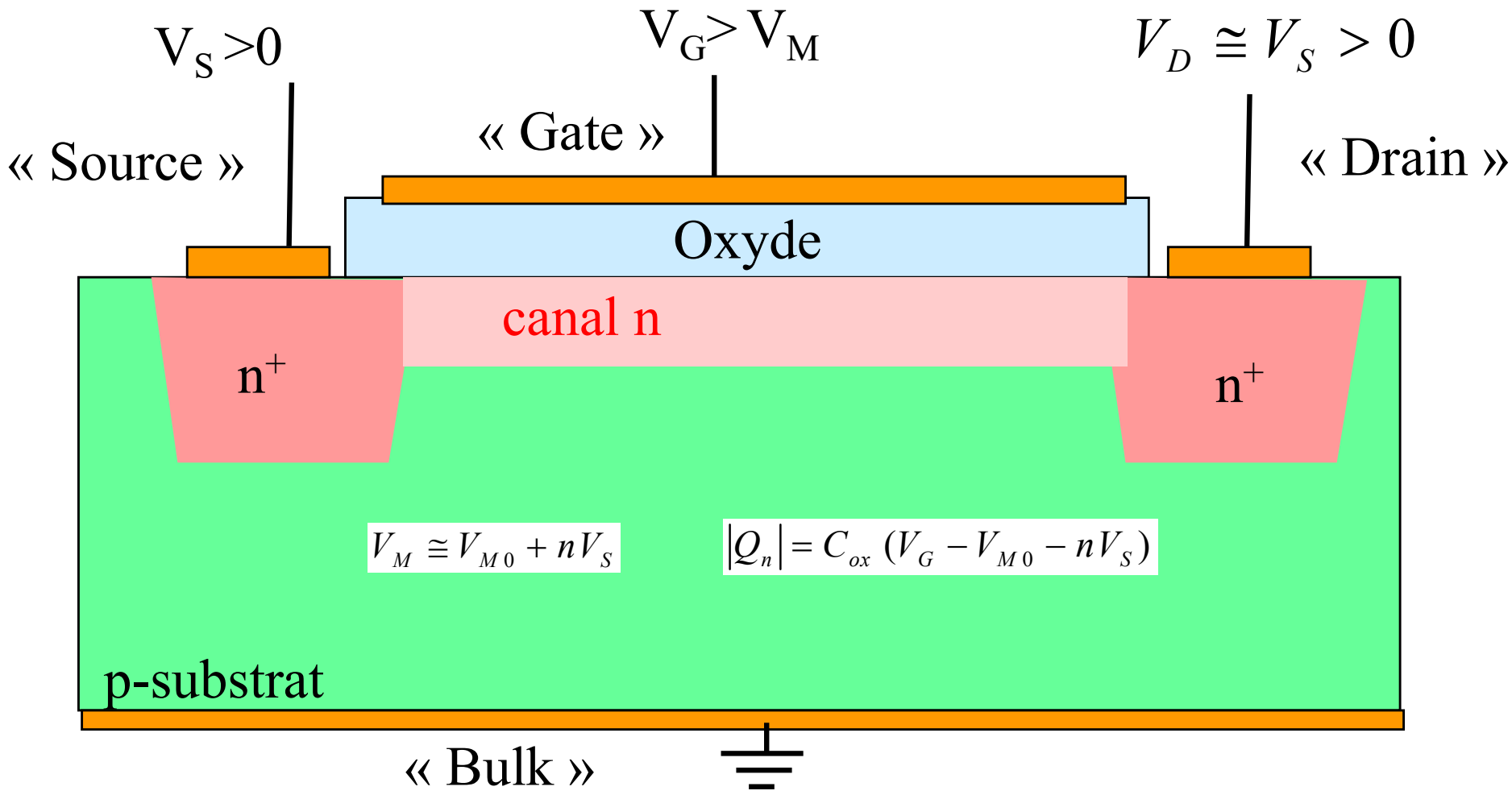

Threshold:

$$V_G - V_{M0} \cong n \cdot (\psi_s - 2\psi_B) \quad \Rightarrow \quad V_M - V_{M0} \cong n \cdot V_S$$

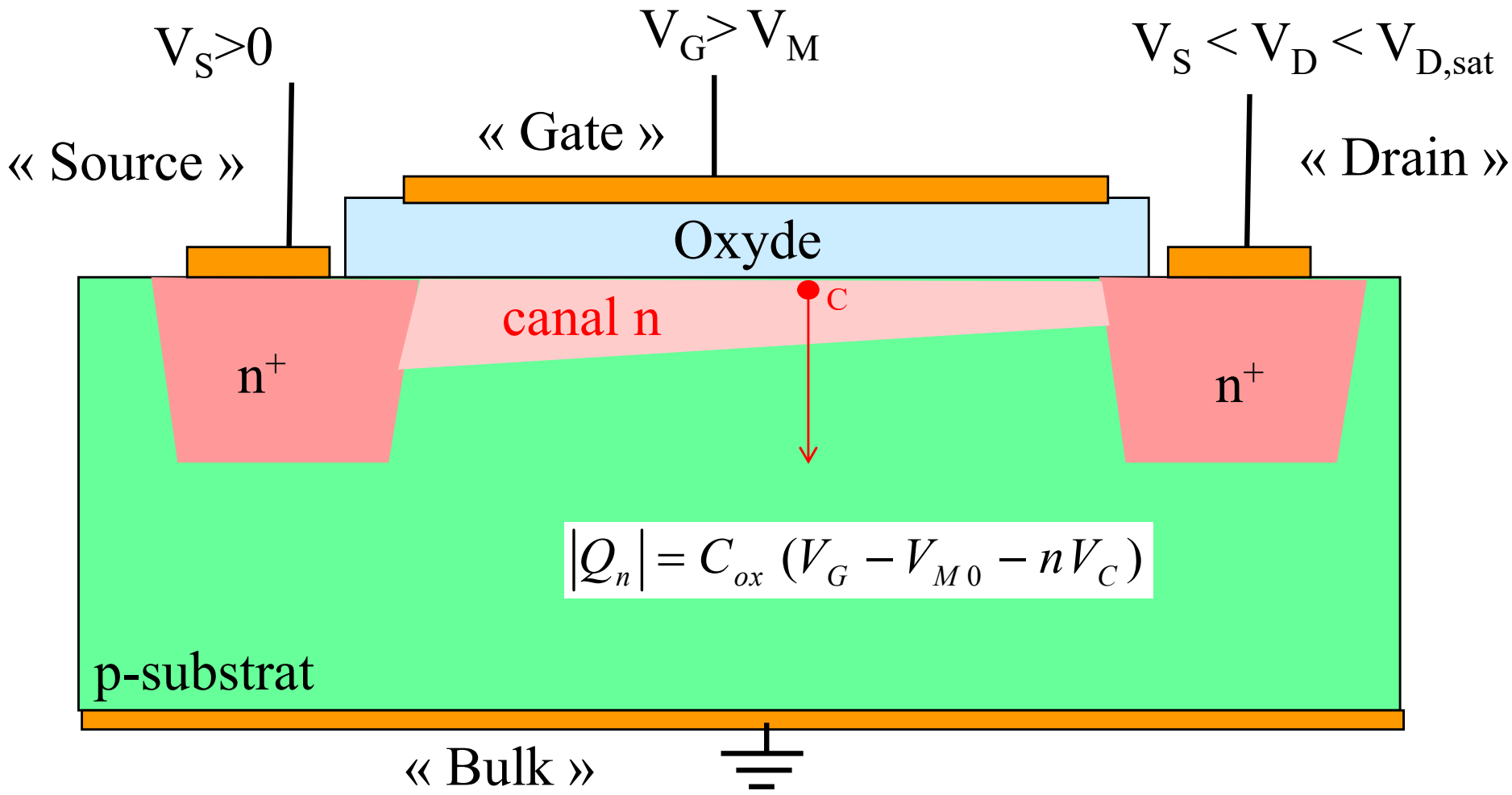
Inversion: $V_G > V_M$

$$Q_n = -C_{ox}(V_G - V_{M0} - nV_S)$$

# Influence de $V_S$

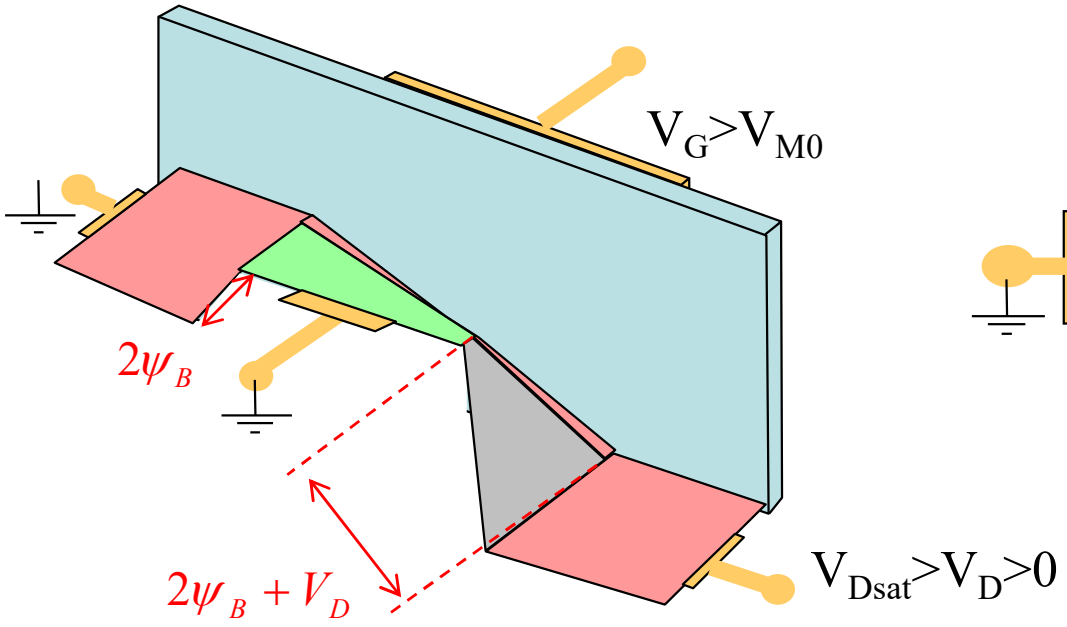


# NMOS en inversion forte, régime ohmique

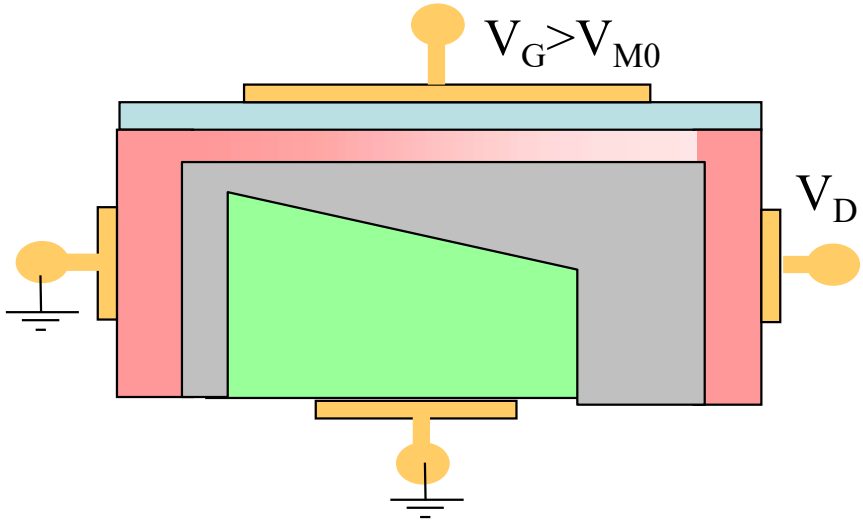


# Régime FET ohmique: vision 3D

Bande de conduction:

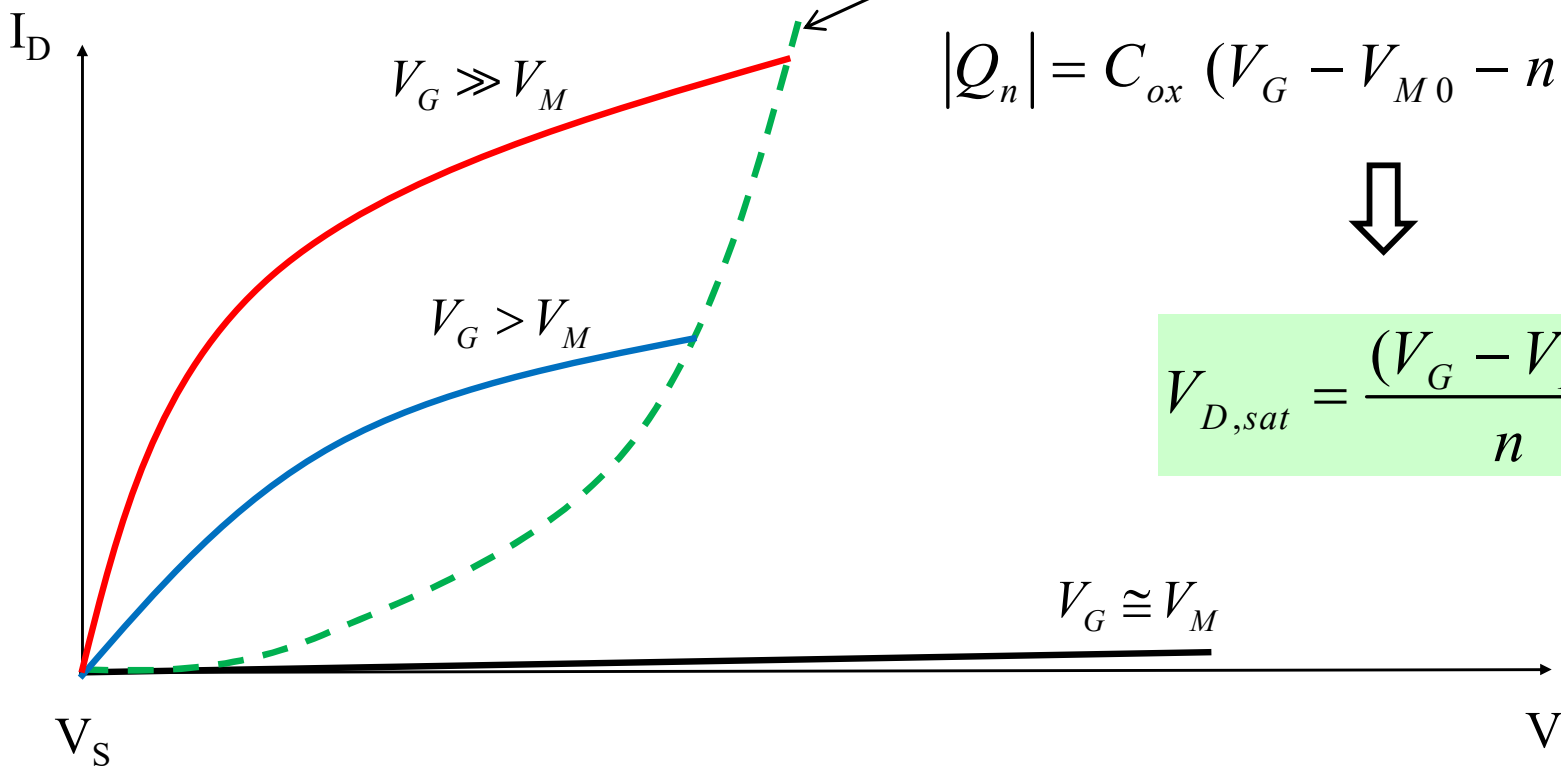



Vue latérale:




Les charges dans le canal diminuent lorsqu'on s'approche du drain

# Régime FET ohmique: courbes caractéristiques




$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_{D,sat}) = 0$$

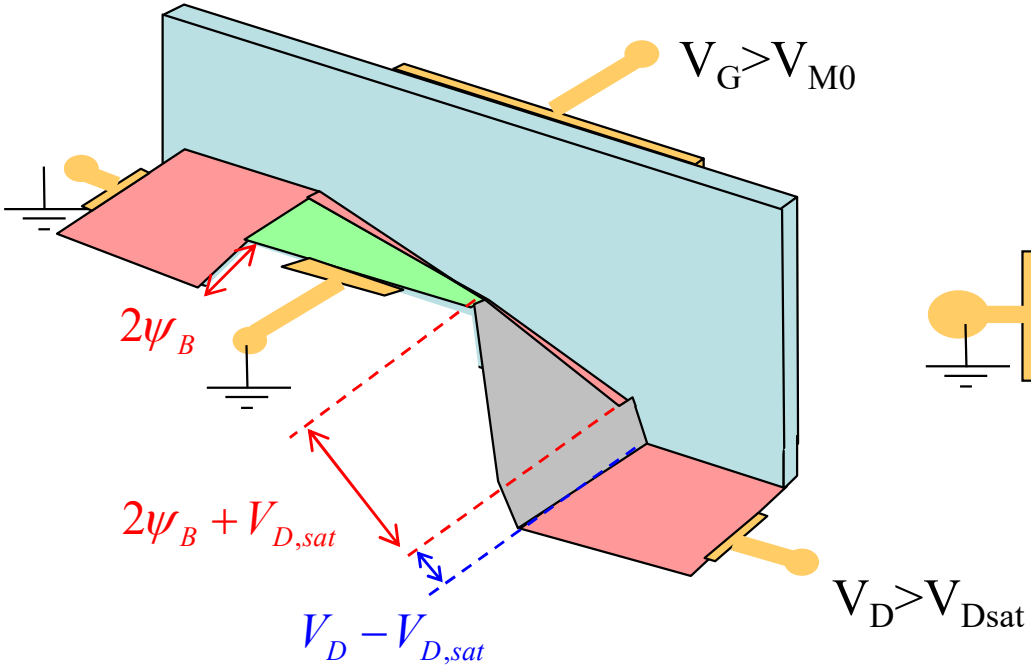
$$\Downarrow$$

$$V_{D,sat} = \frac{(V_G - V_{M0})}{n}$$

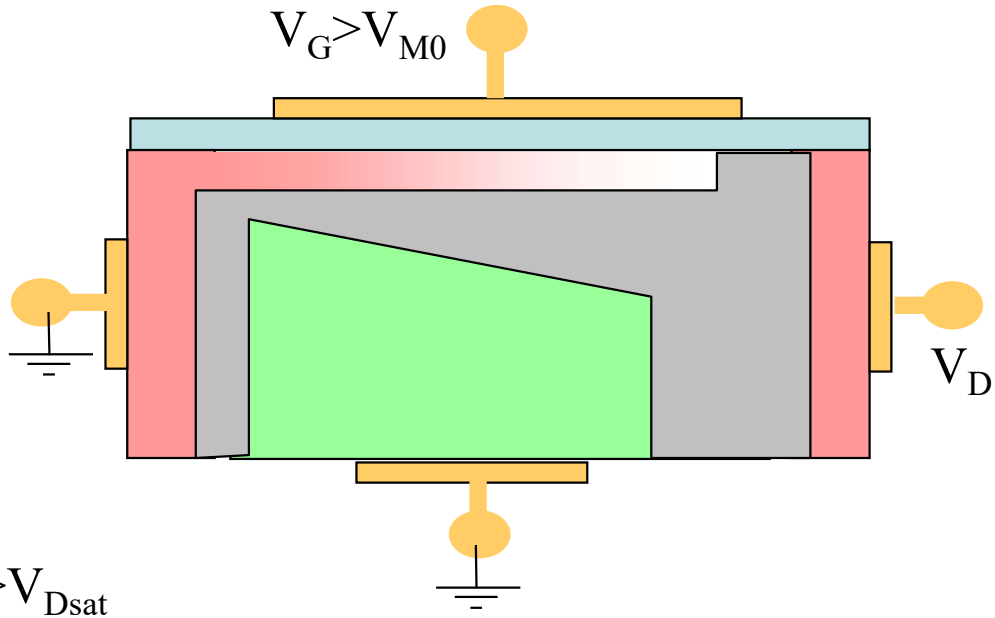
$$V_M \cong V_{M0} + nV_S$$

# Pincement du canal: vision 3D

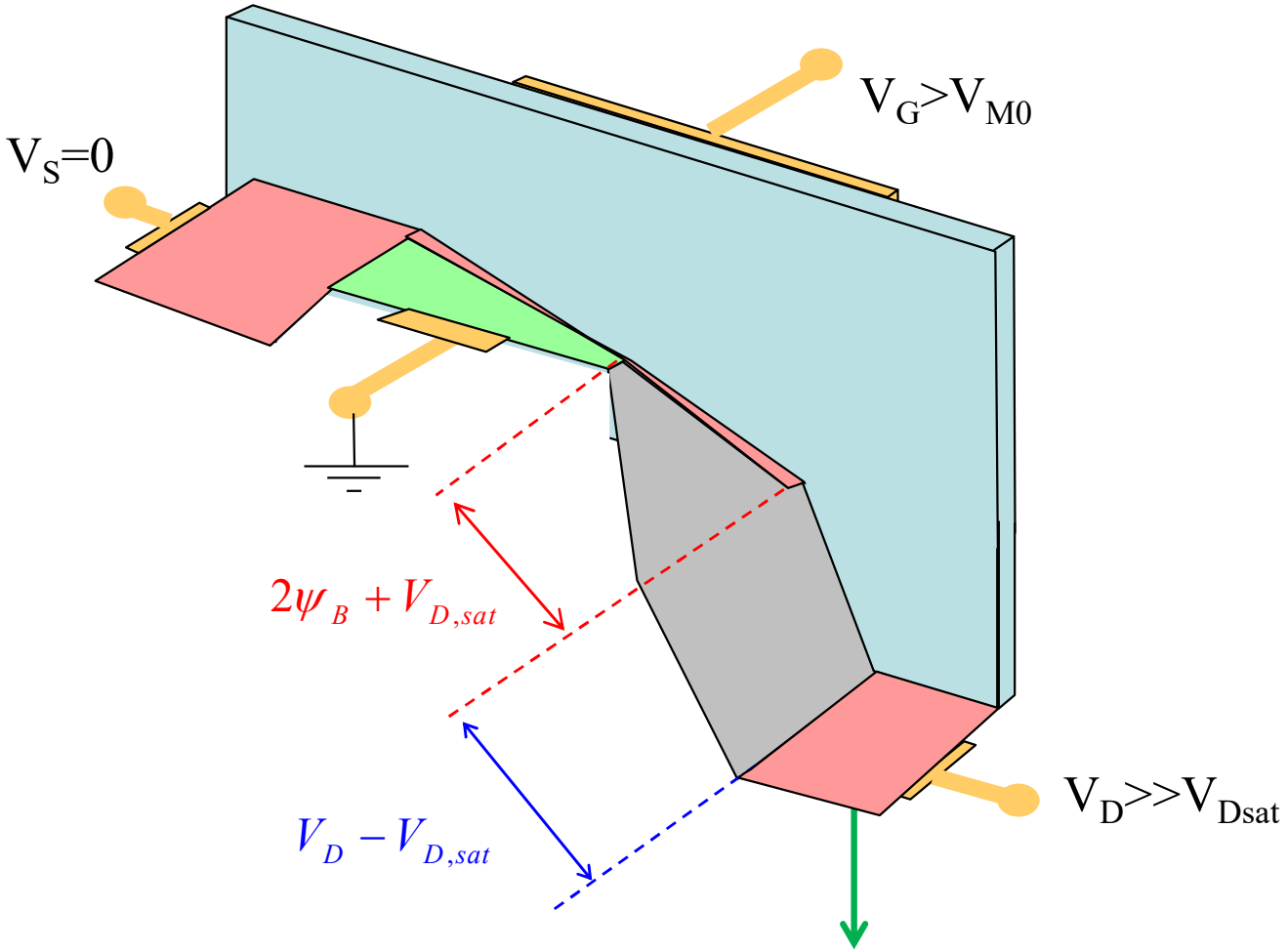
Bande de conduction:



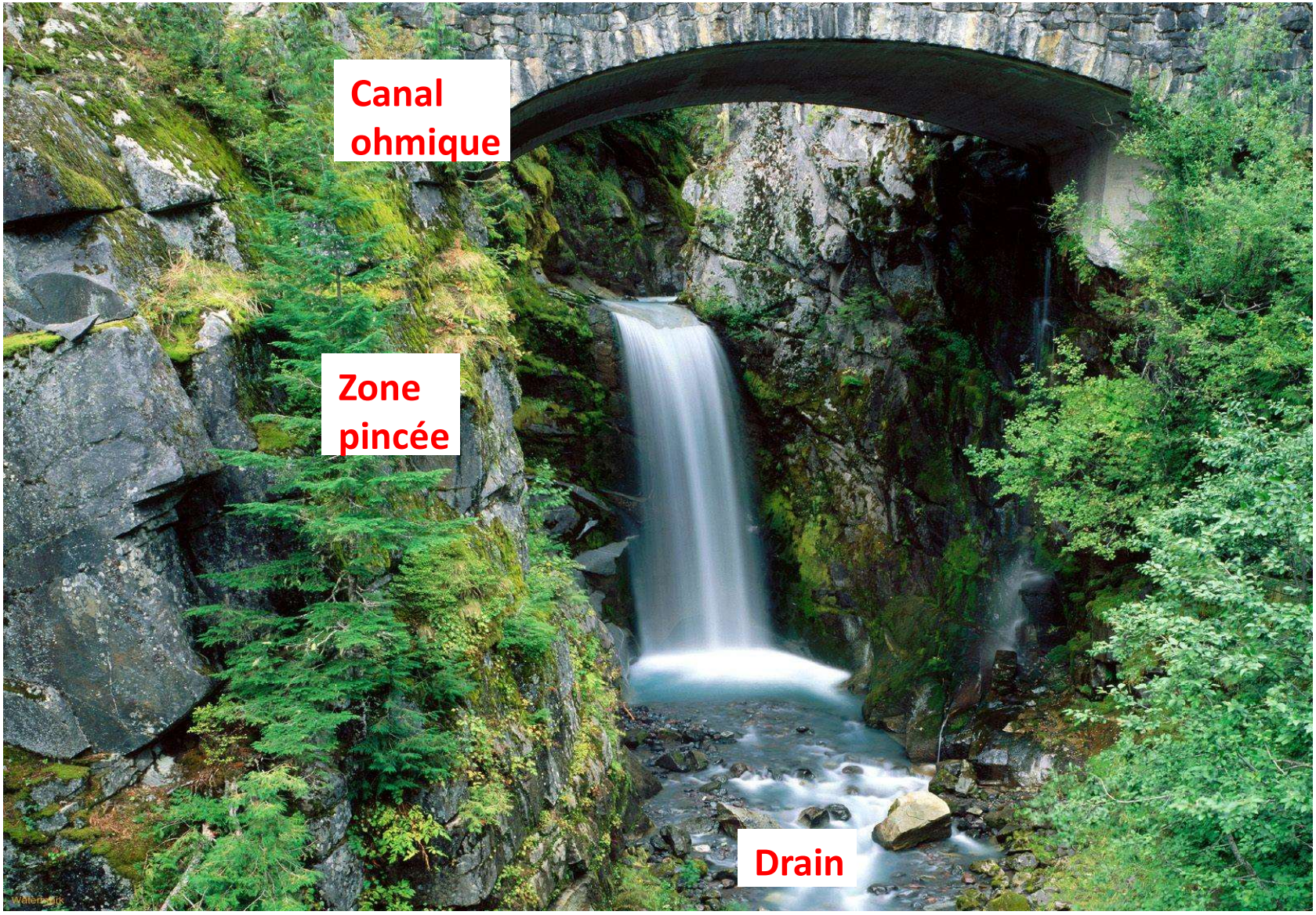

Vue latérale:



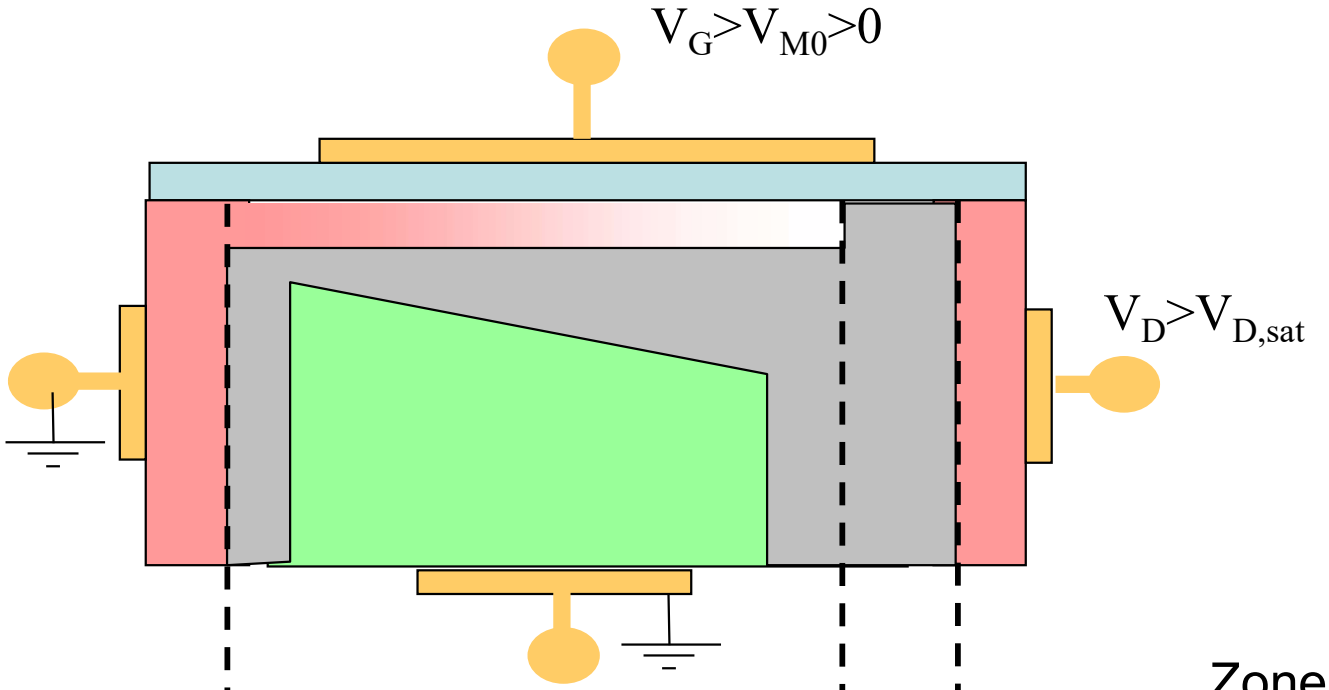
# Régime de saturation



# Pincement du canal NMOS



# Pincement du canal



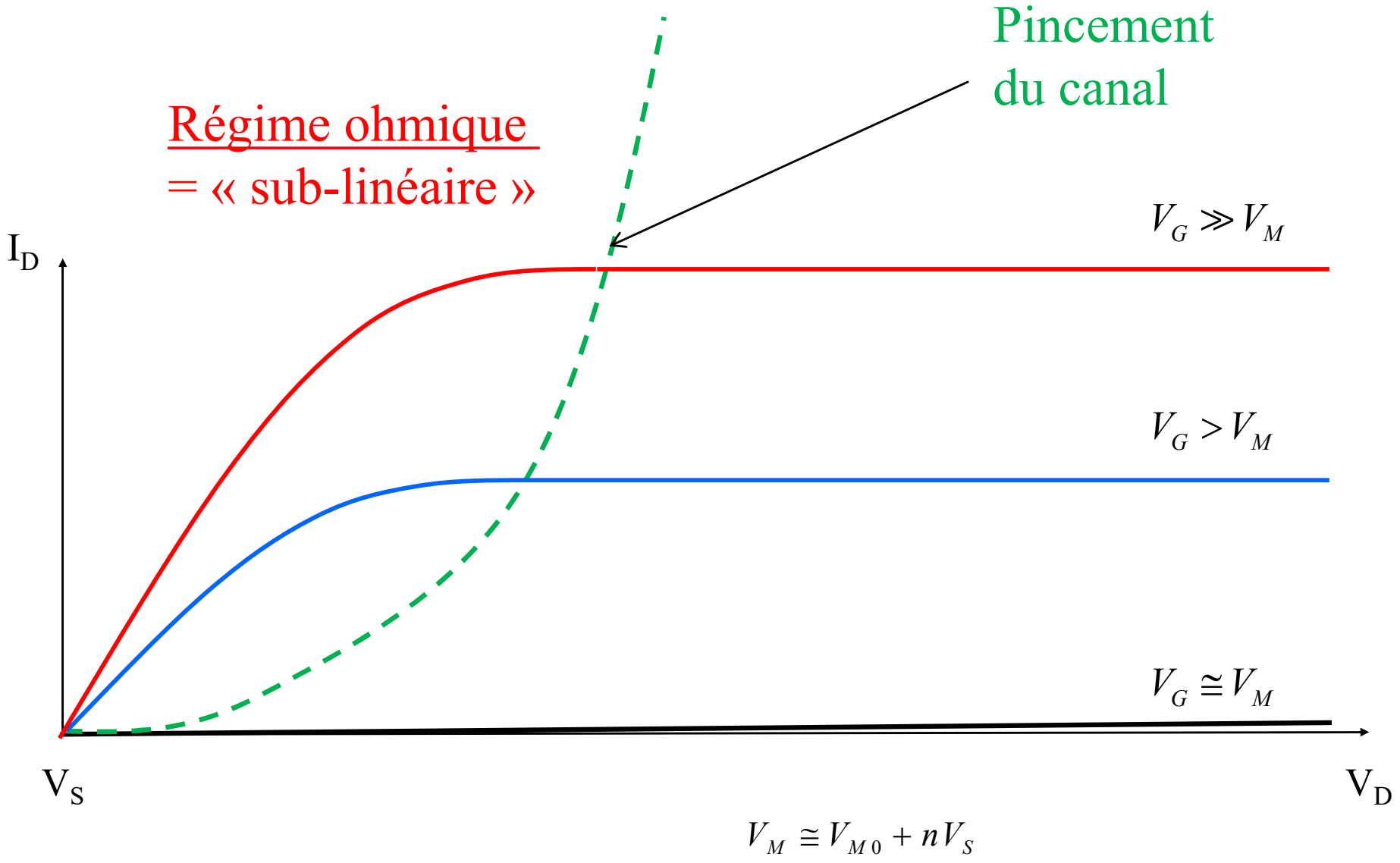

Zone de déplétion
→
«absorbe» l'excès de tension $V_D$-$V_{D,sat}$

Résistance fixe
→
$I_D$ indépendant de $V_D$

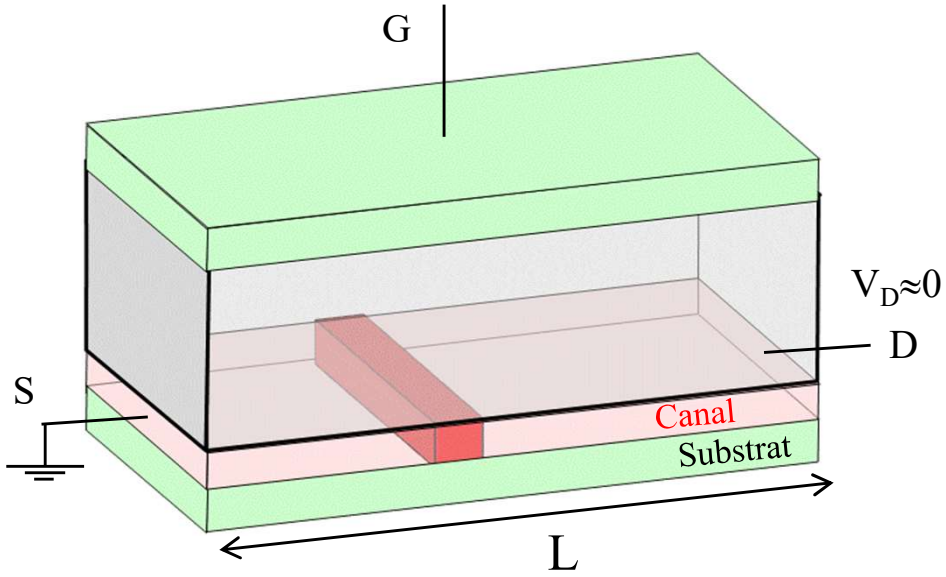
**Chute de tension $V_{D,sat}$**

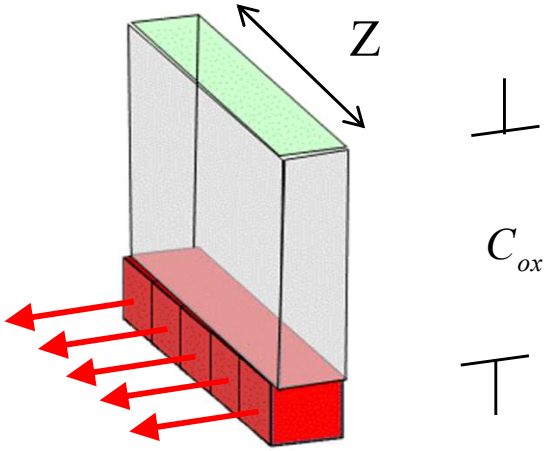
**Chute de tension $V_D$-$V_{D,sat}$**

# Régime FET idéal



# Exercice: calcul simplifié du courant en inversion forte



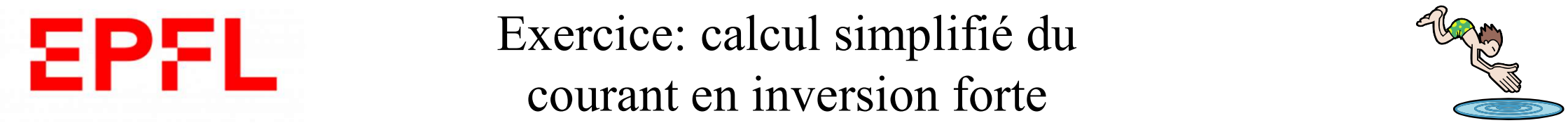




$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_C)$$

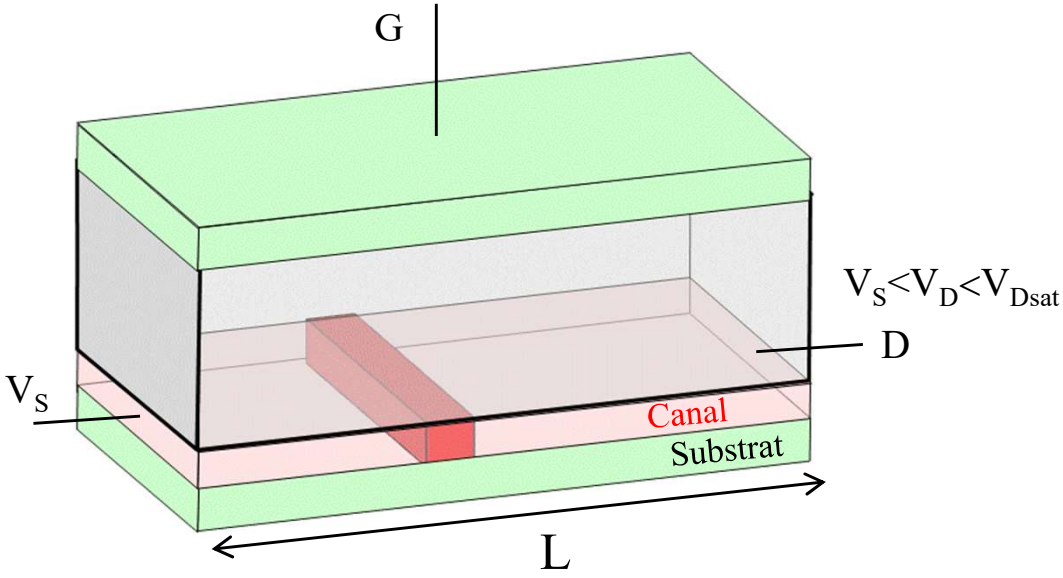
$$\frac{I_D}{Z} = Q_n \,.\, v = \ldots$$

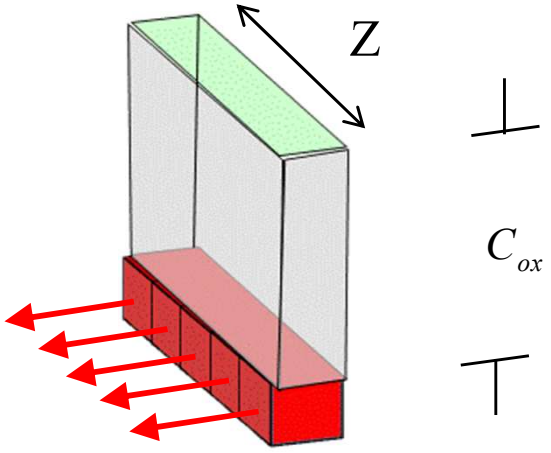
Développez l'expression du courant en considérant la charge et la vitesse moyenne au milieu du canal

# Exercice: calcul simplifié du courant en inversion forte



## A) Régime ohmique



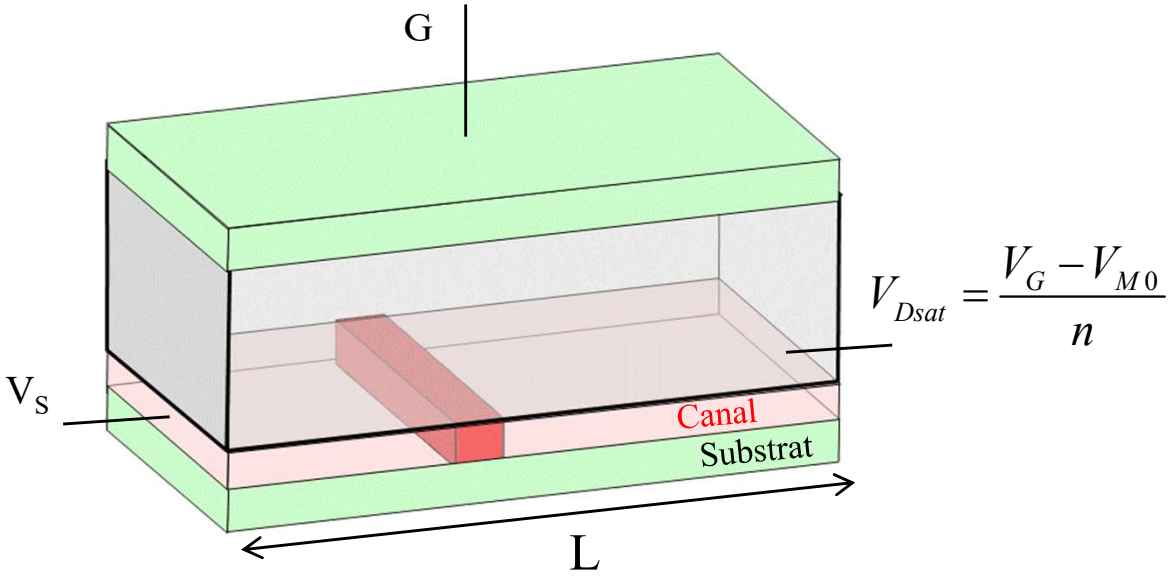



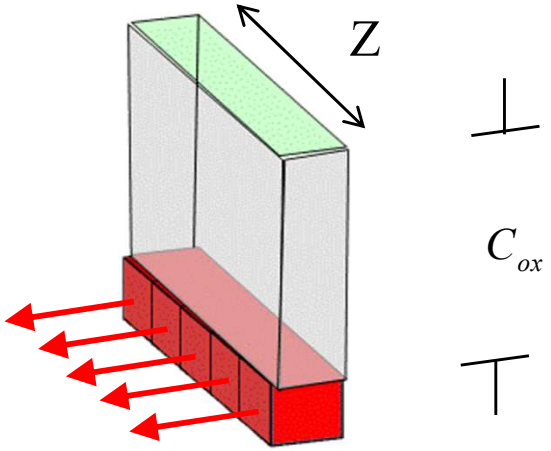

$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_C)$$

$$\frac{I_D}{Z} = \left(\frac{Q_{n,S} + Q_{n,D}}{2}\right)\cdot\left(\mu_n\left|\vec{E}\right|\right) = C_{ox}\left(V_G - V_{M0} - n\frac{V_D + V_S}{2}\right)\cdot\left(\mu_n\frac{V_D - V_S}{L}\right)$$

# Exercice: calcul simplifié du courant en inversion forte

## B) Régime de saturation



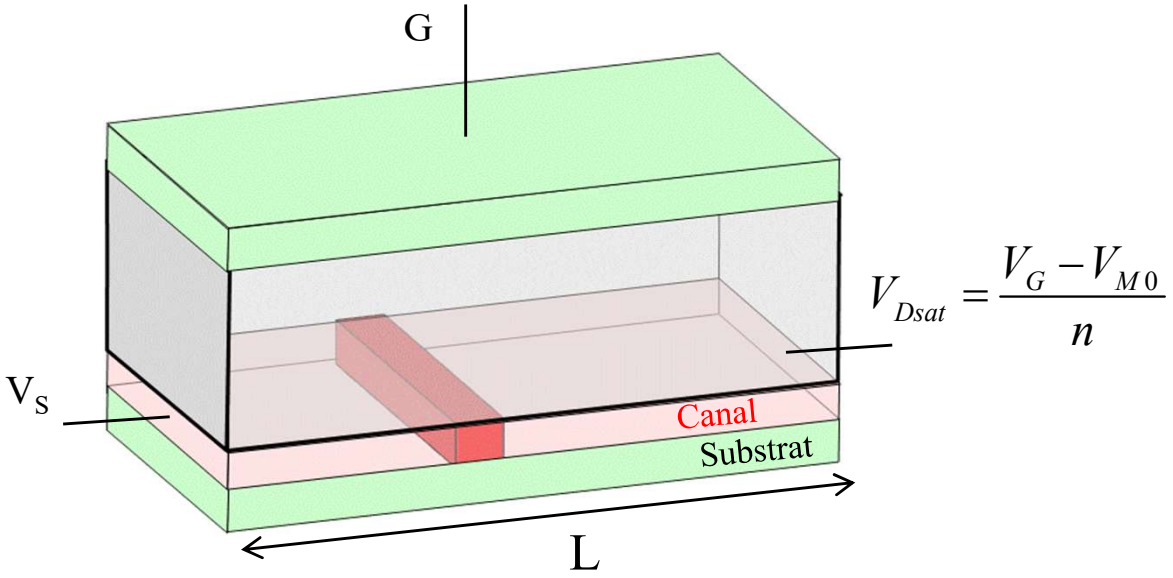



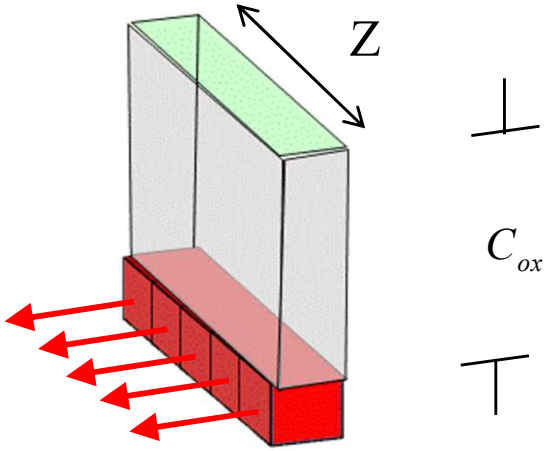

$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_C)$$

$$\frac{I_D}{Z} = \left(\frac{Q_{n,S} + Q_{n,D}}{2}\right)\cdot\left(\mu_n\left|\vec{E}\right|\right) = \frac{C_{ox}\left(V_G - V_{M0} - nV_S\right)}{2}\cdot\left(\mu_n\frac{V_{D,sat} - V_S}{L}\right)$$

# Exercice: calcul simplifié du courant en inversion forte

## B) Régime de saturation

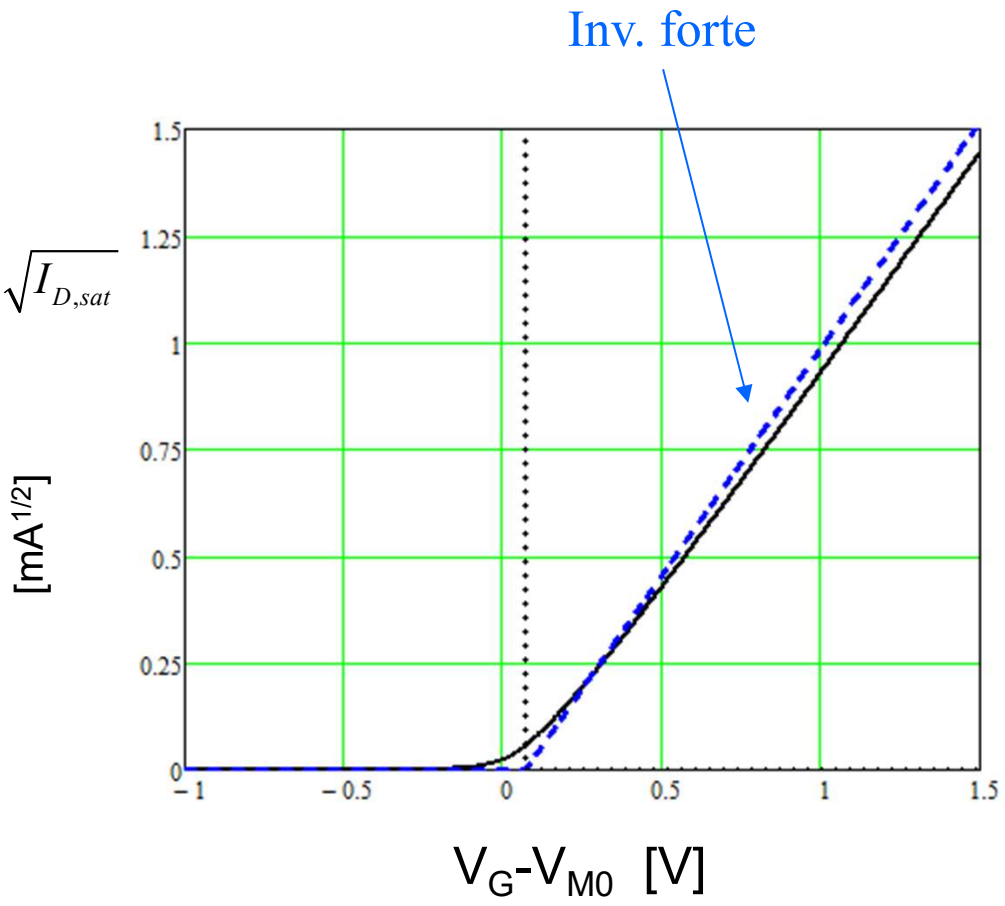


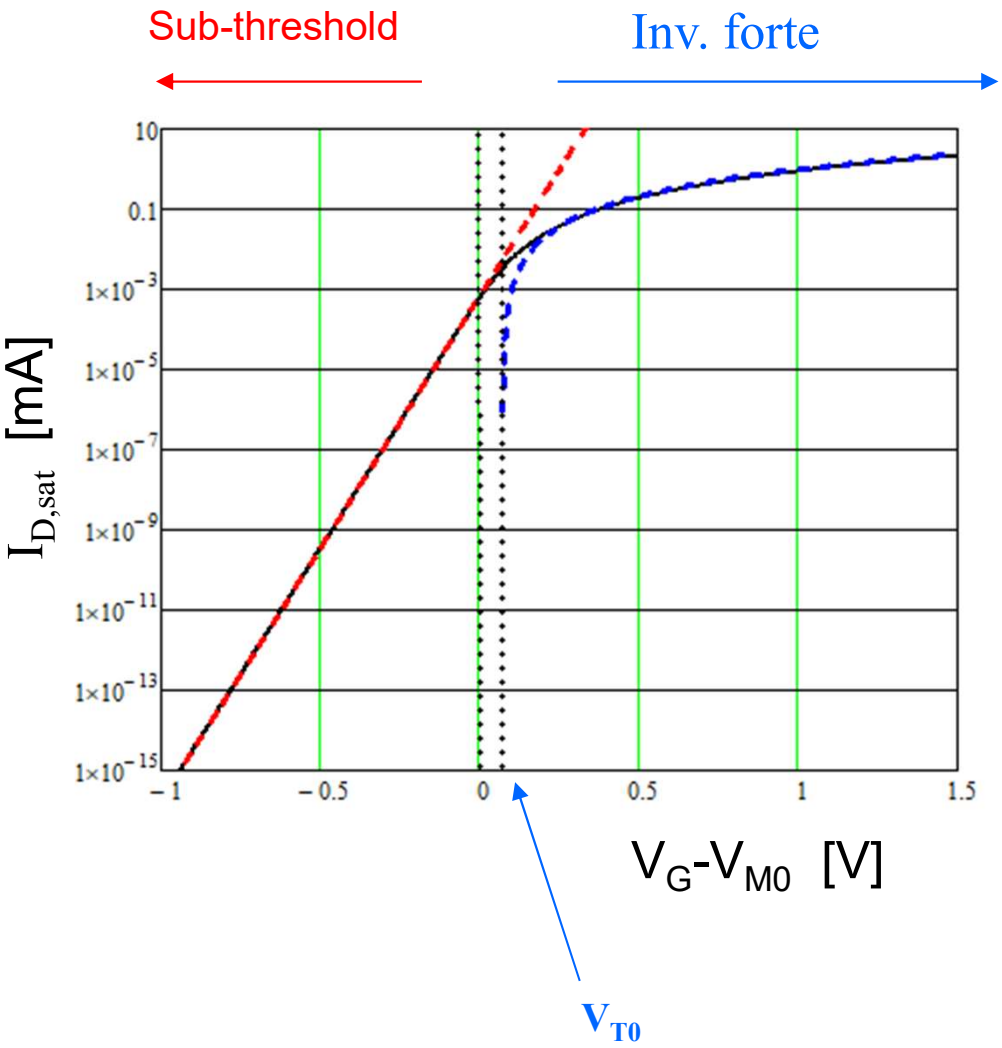




$$|Q_n| = C_{ox}\,(V_G - V_{M0} - nV_C)$$

$$\frac{I_D}{Z} = \left(\frac{Q_{n,S} + Q_{n,D}}{2}\right)\cdot\left(\mu_n\left|\vec{E}\right|\right) \quad = \mu_n C_{ox}\,\frac{\left(V_G - V_{M0} - nV_S\right)^2}{2\cdot n\cdot L}$$

# Inversion forte en saturation ($V_D > V_{D,sat}$)

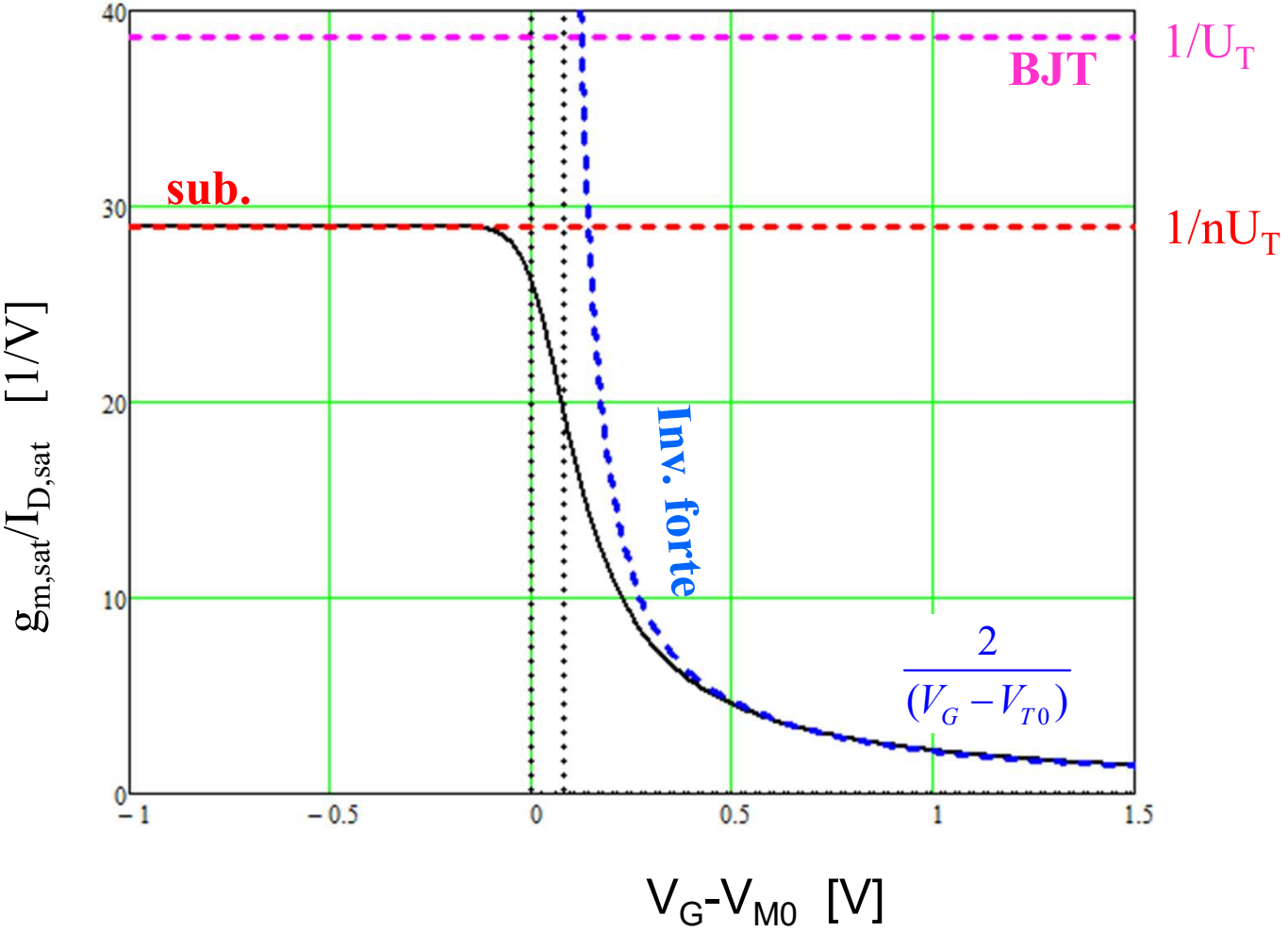



$C_{ox}$=3fF/um$^2$
W/L=10
T=300 K

$u_n$=1000cm$^2$/V.s
n=4/3

# Transconductance en saturation: $g_m/I_D$



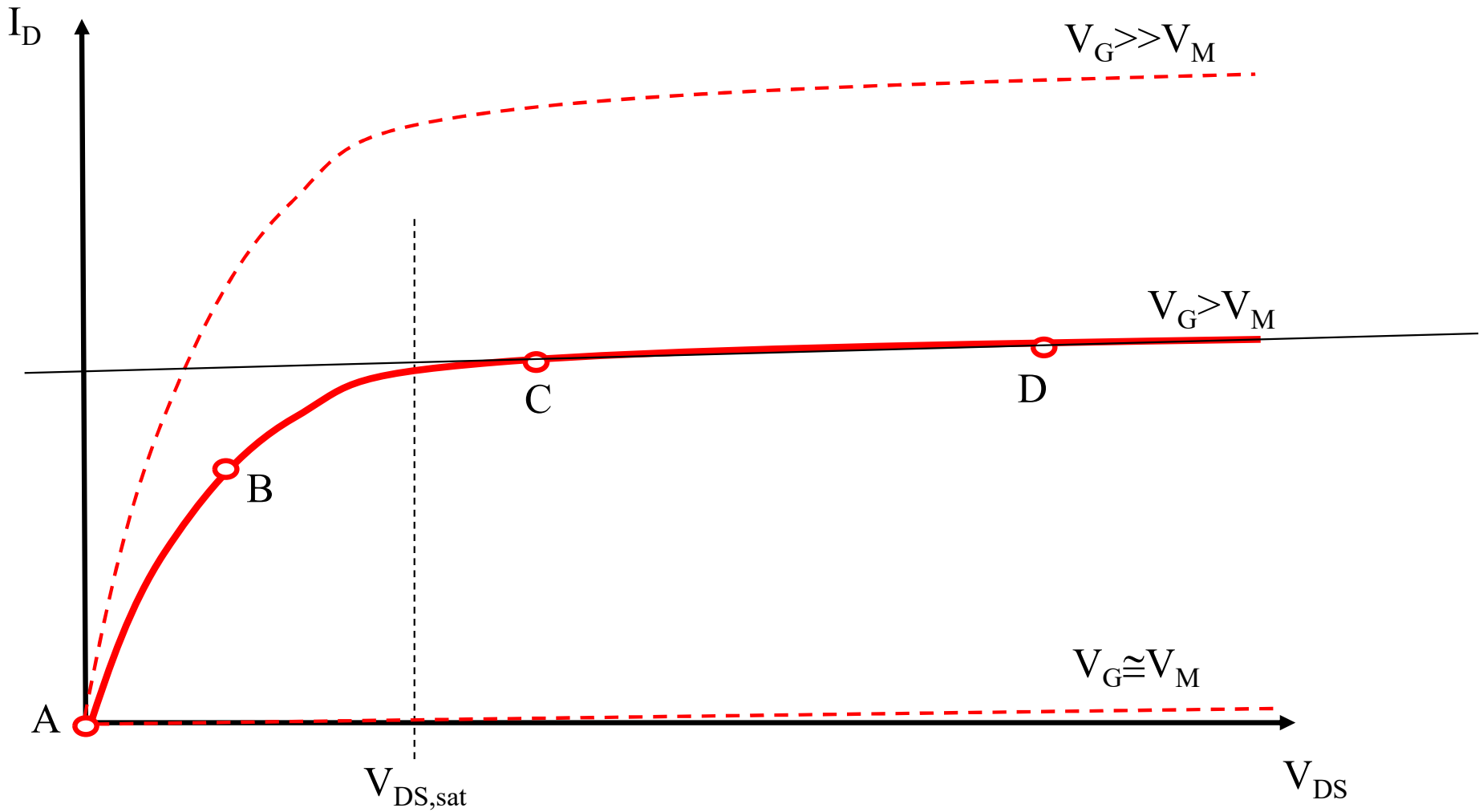

Transconductance définition

$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G}$$

$C_{ox}$=3fF/um$^2$
W/L=10
T=300 K

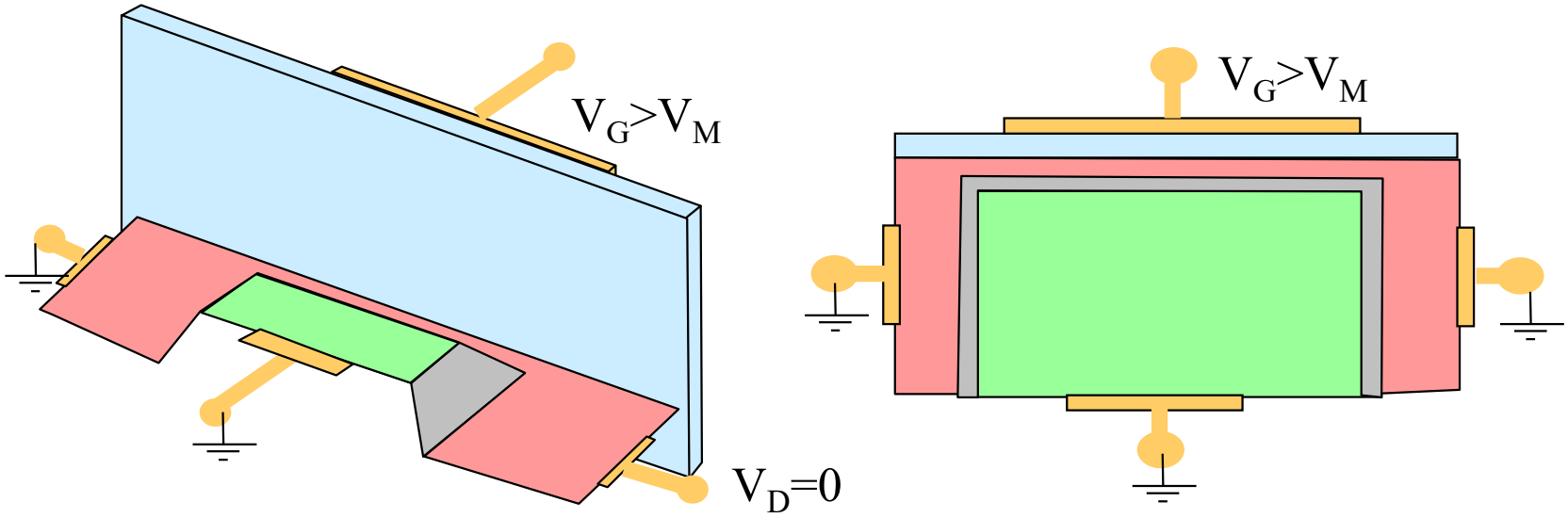
$u_n$=1000cm$^2$/V.s
n=4/3

# Résumé NMOS : comportement en régime FET en fonction de la tension de drain

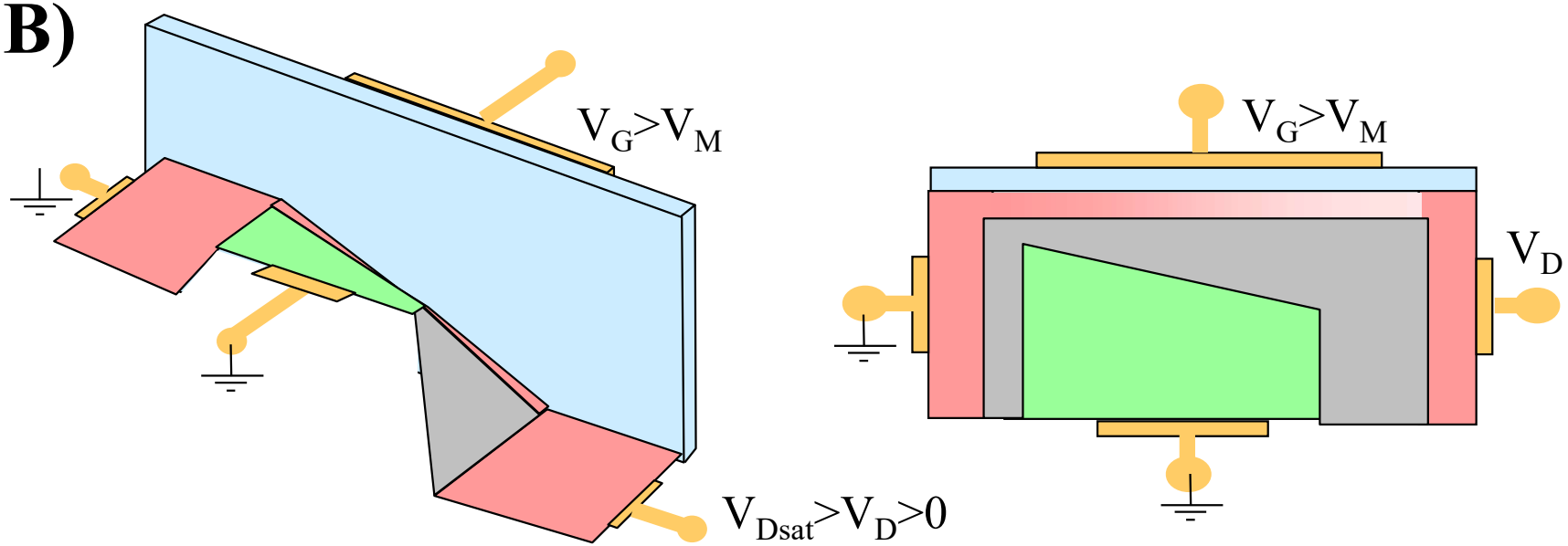


# Résumé NMOS (1)

**A)**

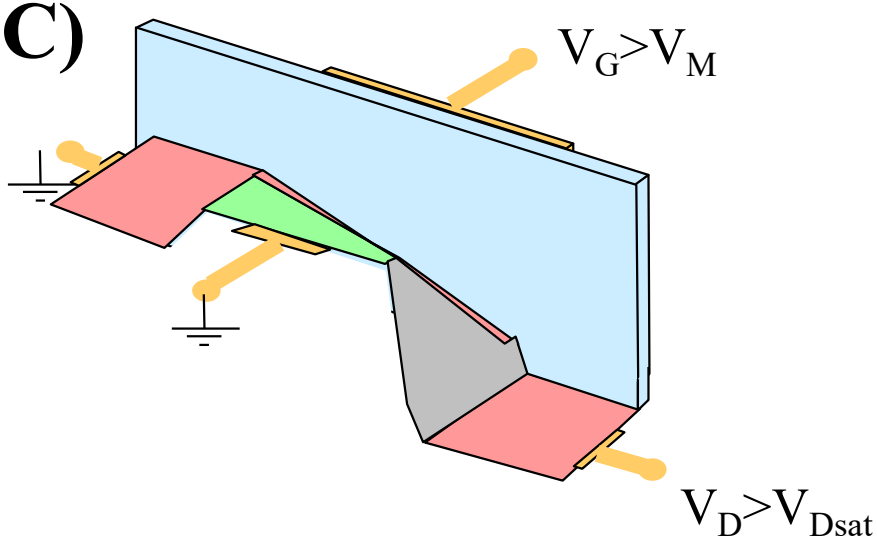


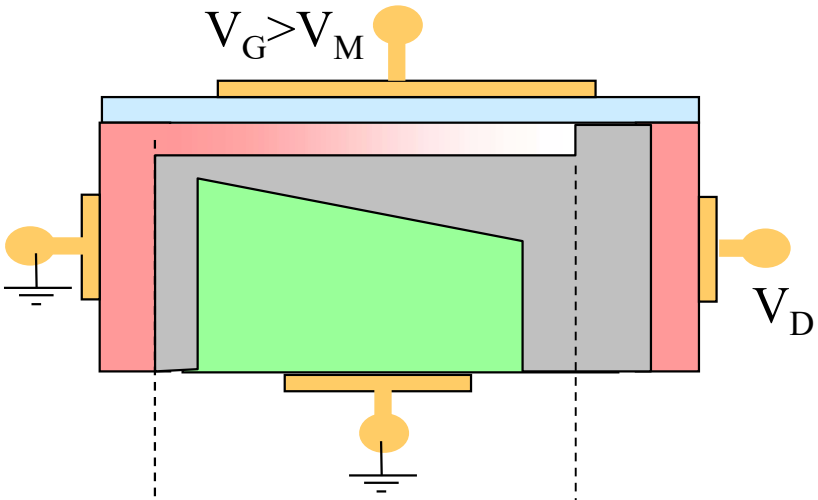

**B)**



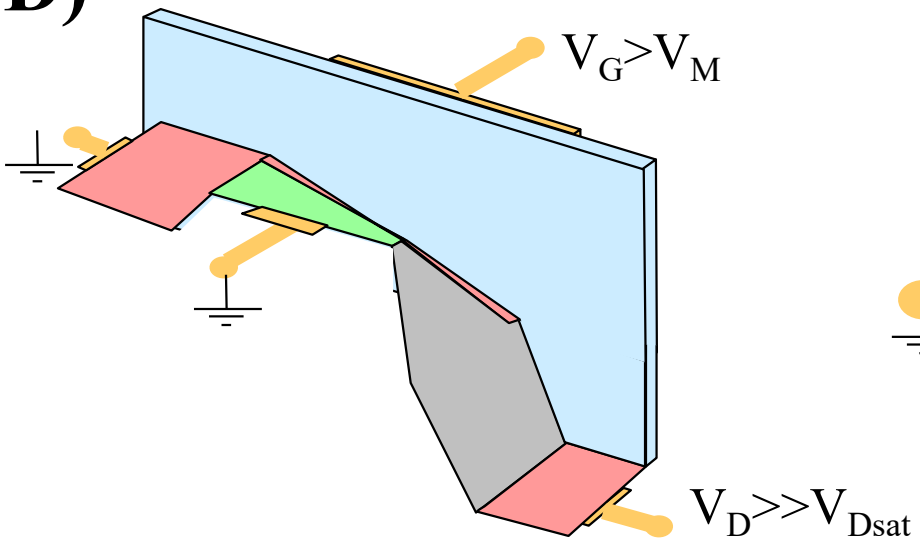
# Résumé NMOS (2)

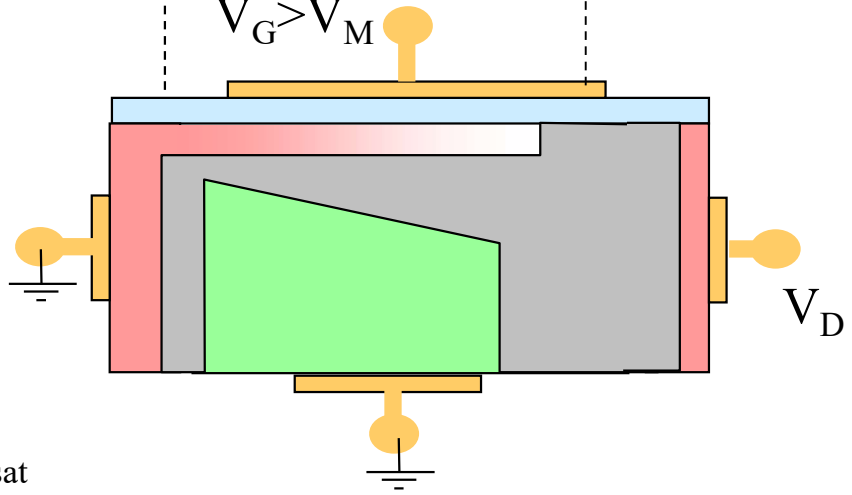
**C)**



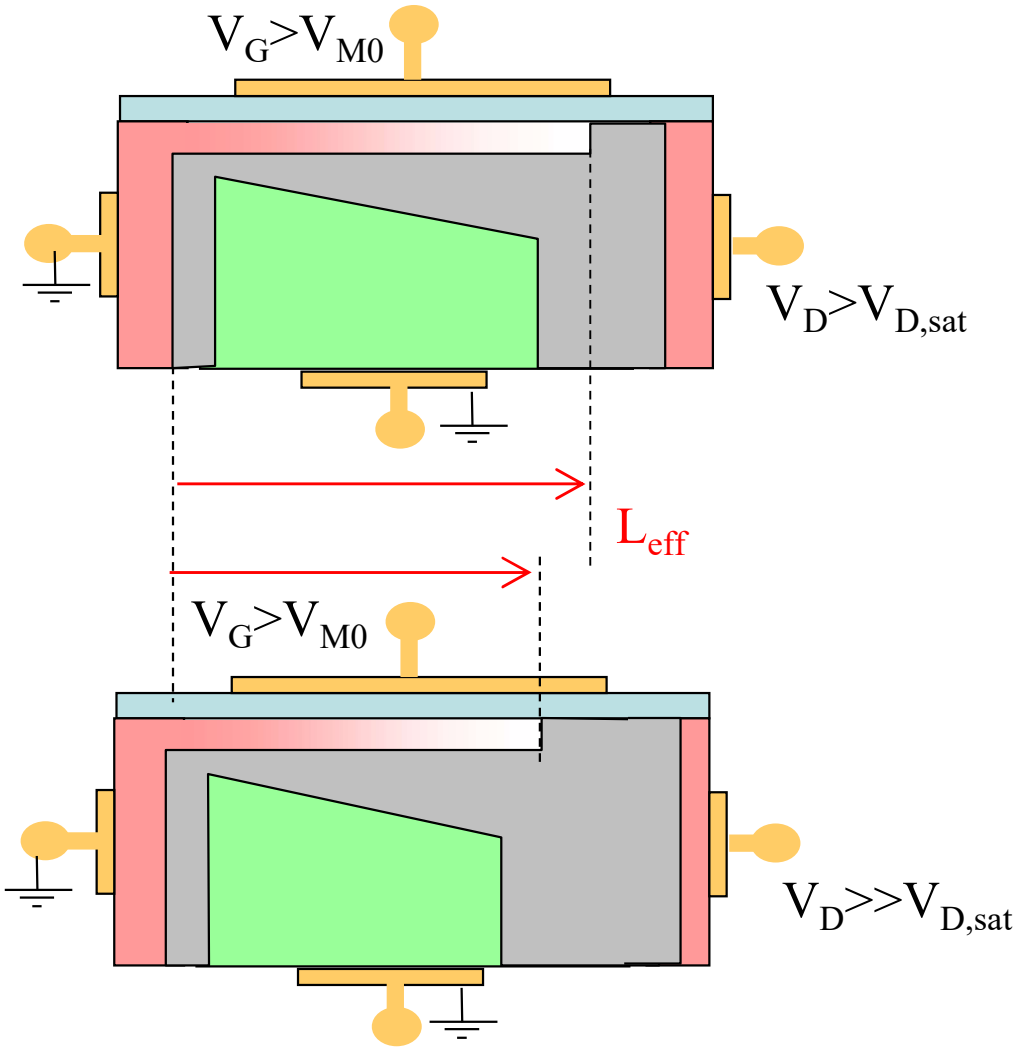




**D)**



# Modulation de la longueur du canal



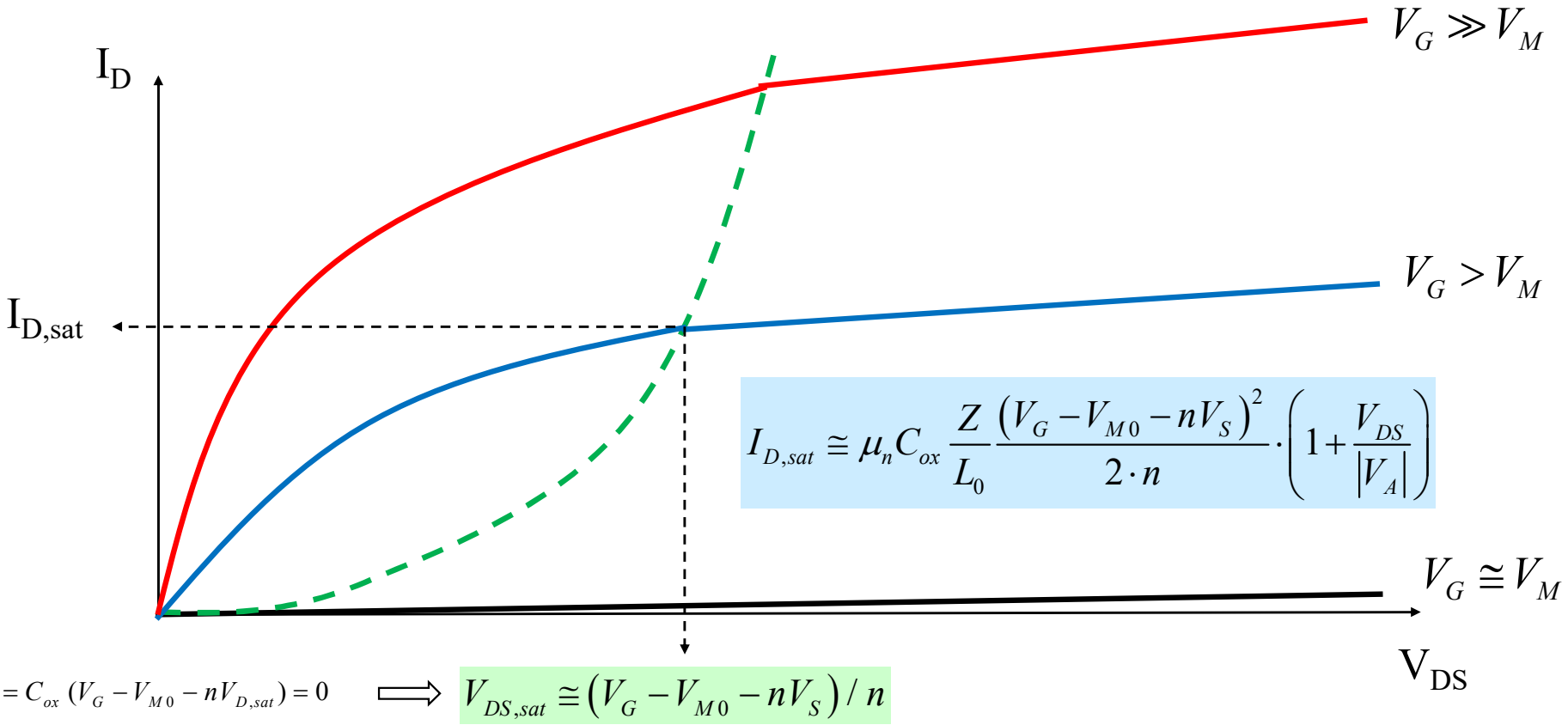

Le canal se rétrécit lentement avec l'augmentation de la tension de drain $V_D$.

→ Le courant de drain augmente légèrement

$$I_{D,sat} \approx \frac{1}{L_{eff}} = \frac{1}{L_0} \cdot \left(1 + \frac{V_{DS}}{|V_A|}\right)$$

# Courbes de sortie en mode FET avec modulation de la longueur du canal

$$\frac{g_{m,sat}}{I_{D,sat}} \equiv \frac{1}{I_{D,sat}} \frac{\partial I_{D,sat}}{\partial V_G} \cong \frac{2}{(V_G - V_{M0} - nV_S)}$$




$$I_{D,sat} \cong \mu_n C_{ox} \frac{Z}{L_0} \frac{(V_G - V_{M0} - nV_S)^2}{2 \cdot n} \cdot \left(1 + \frac{V_{DS}}{|V_A|}\right)$$

$$|Q_{n,D}| = C_{ox}(V_G - V_{M0} - nV_{D,sat}) = 0 \quad \Longrightarrow \quad V_{DS,sat} \cong (V_G - V_{M0} - nV_S)/n$$

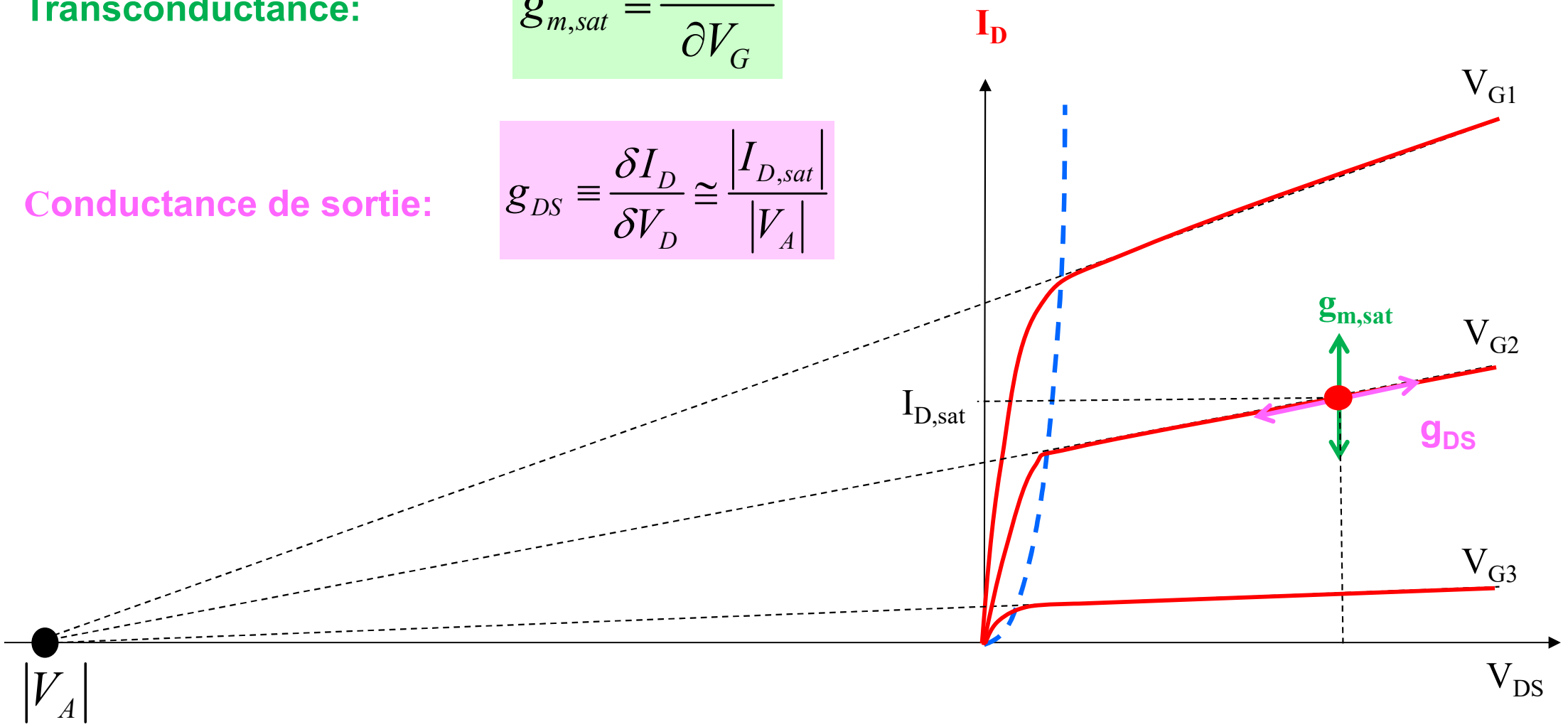
# 10.5: circuit petit signaux : Conductances en mode actif

**Transconductance:**

$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G}$$

**Conductance de sortie:**

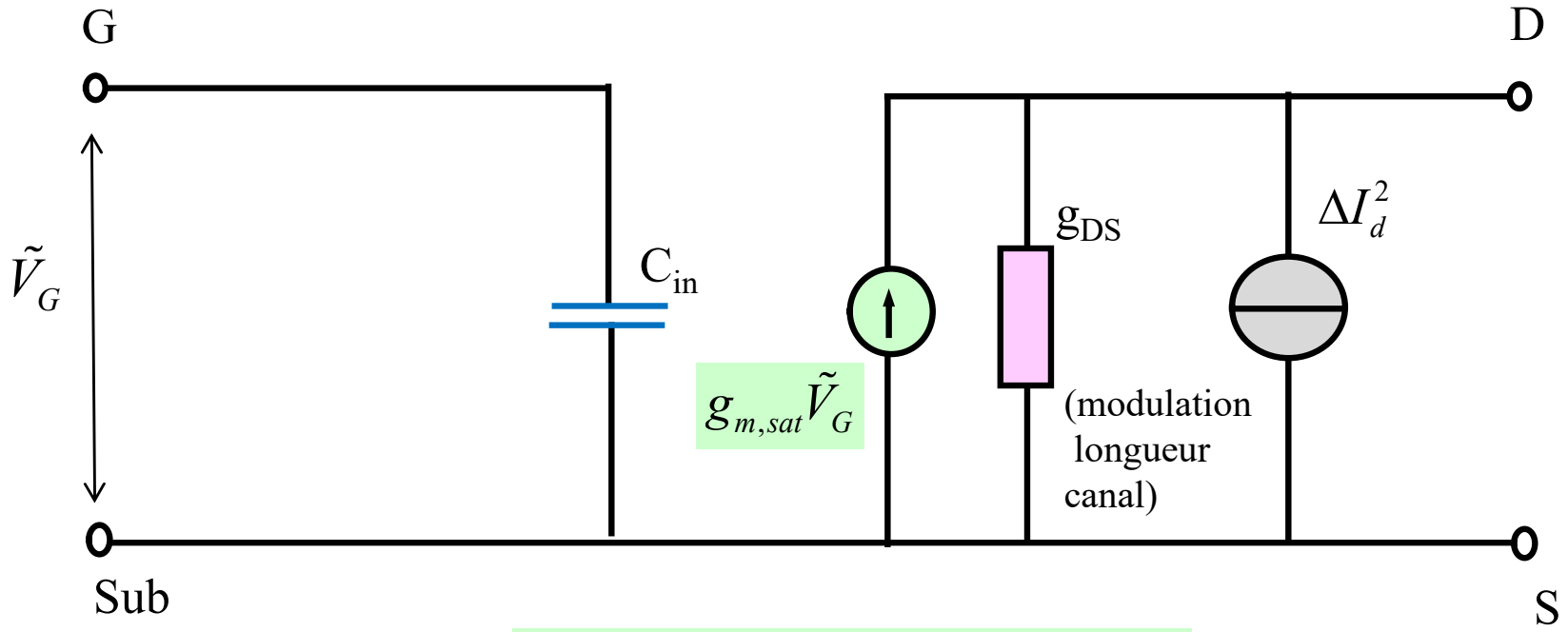
$$g_{DS} \equiv \frac{\delta I_D}{\delta V_D} \cong \frac{|I_{D,sat}|}{|V_A|}$$



# Circuit petits signaux simplifié

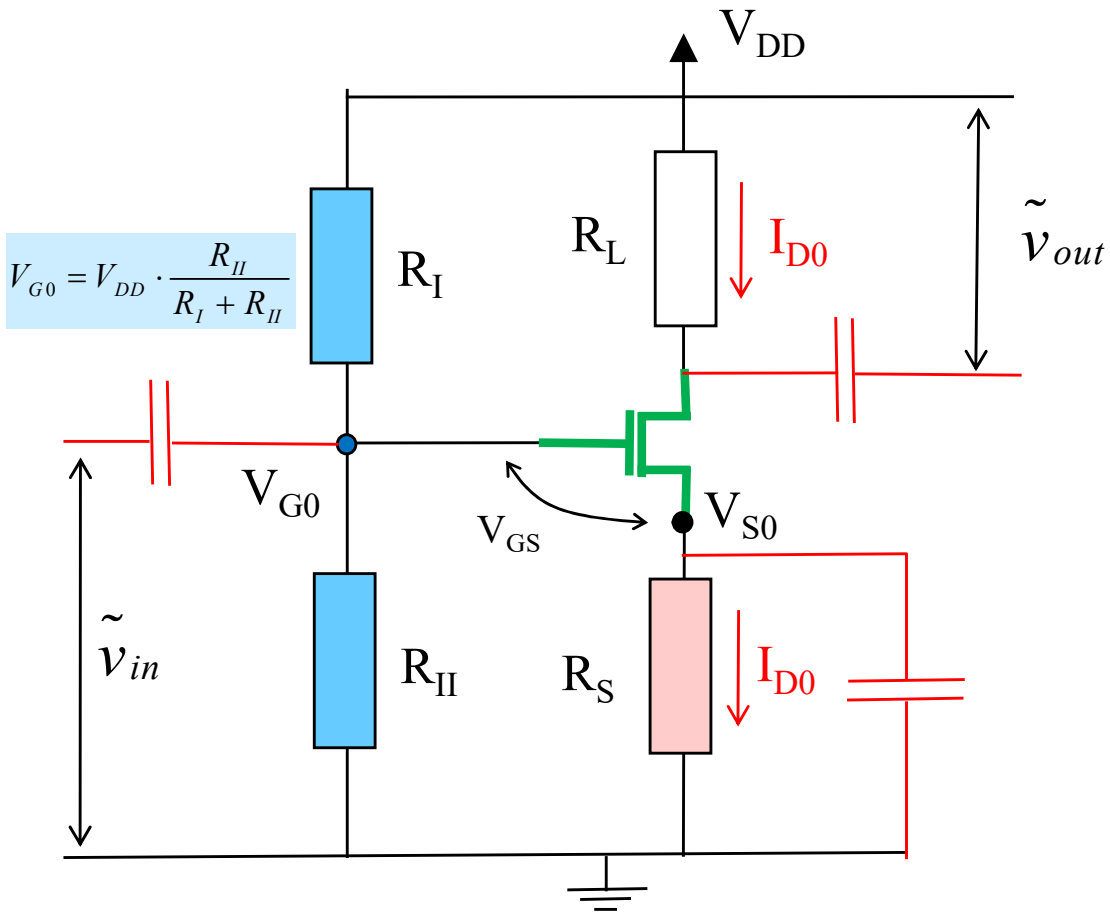
$$C_{in} \cong (Z \cdot L) \cdot \overline{C}_{ox}$$

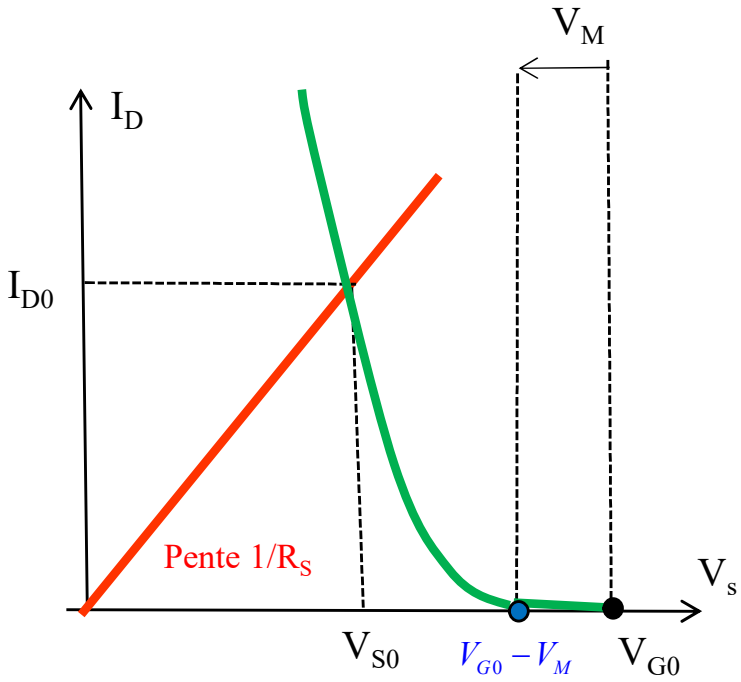
$$g_{DS} \equiv \frac{\delta I_D}{\delta V_D} \cong \frac{|I_{D,sat}|}{|V_A|}$$




$$g_{m,sat} \equiv \frac{\partial I_{D,sat}}{\partial V_G} = I_{D,sat} \cdot \frac{2}{V_G - V_{M0} - nV_S}$$

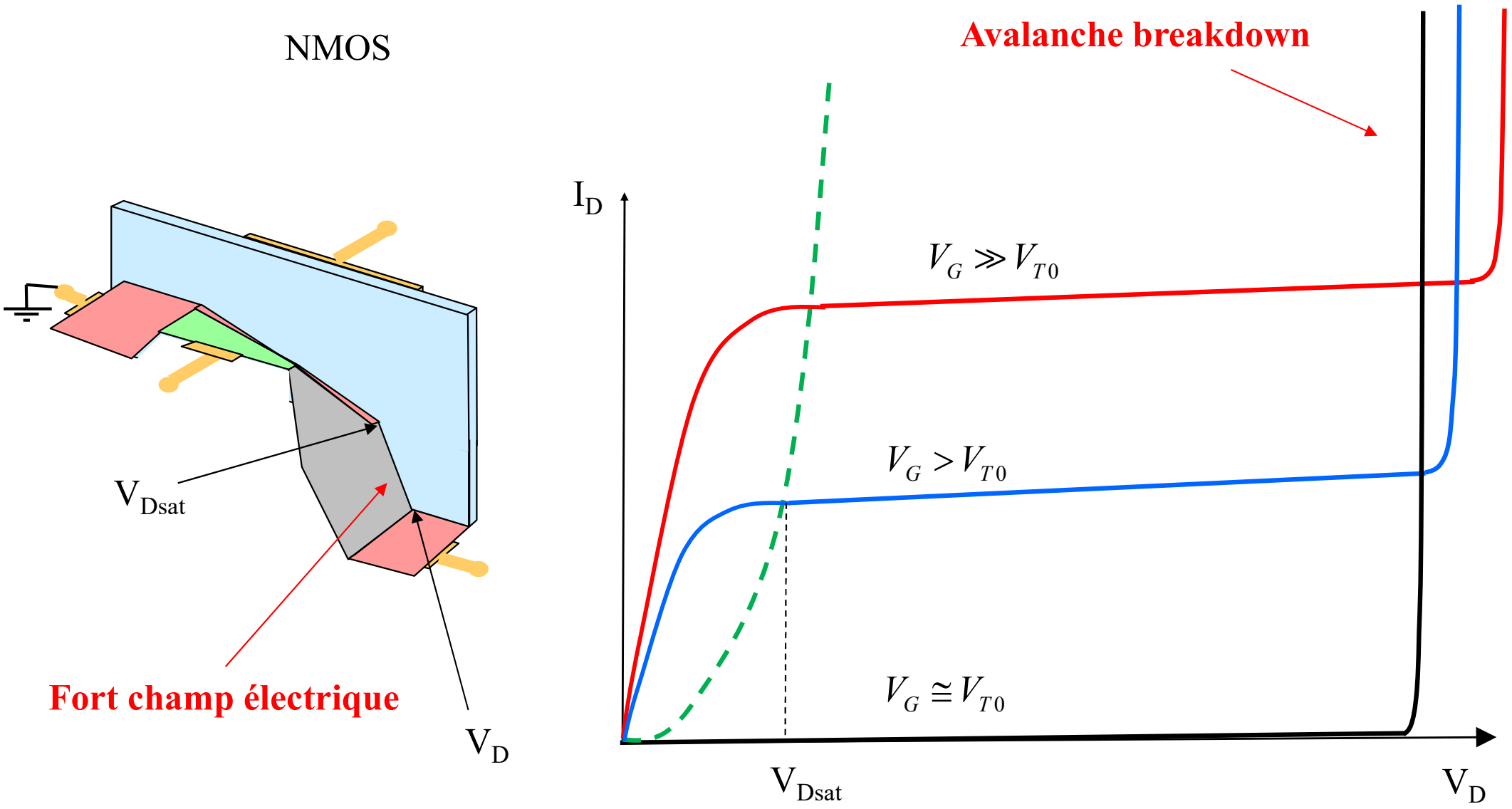
# Polarisation du NMOS: point de travail



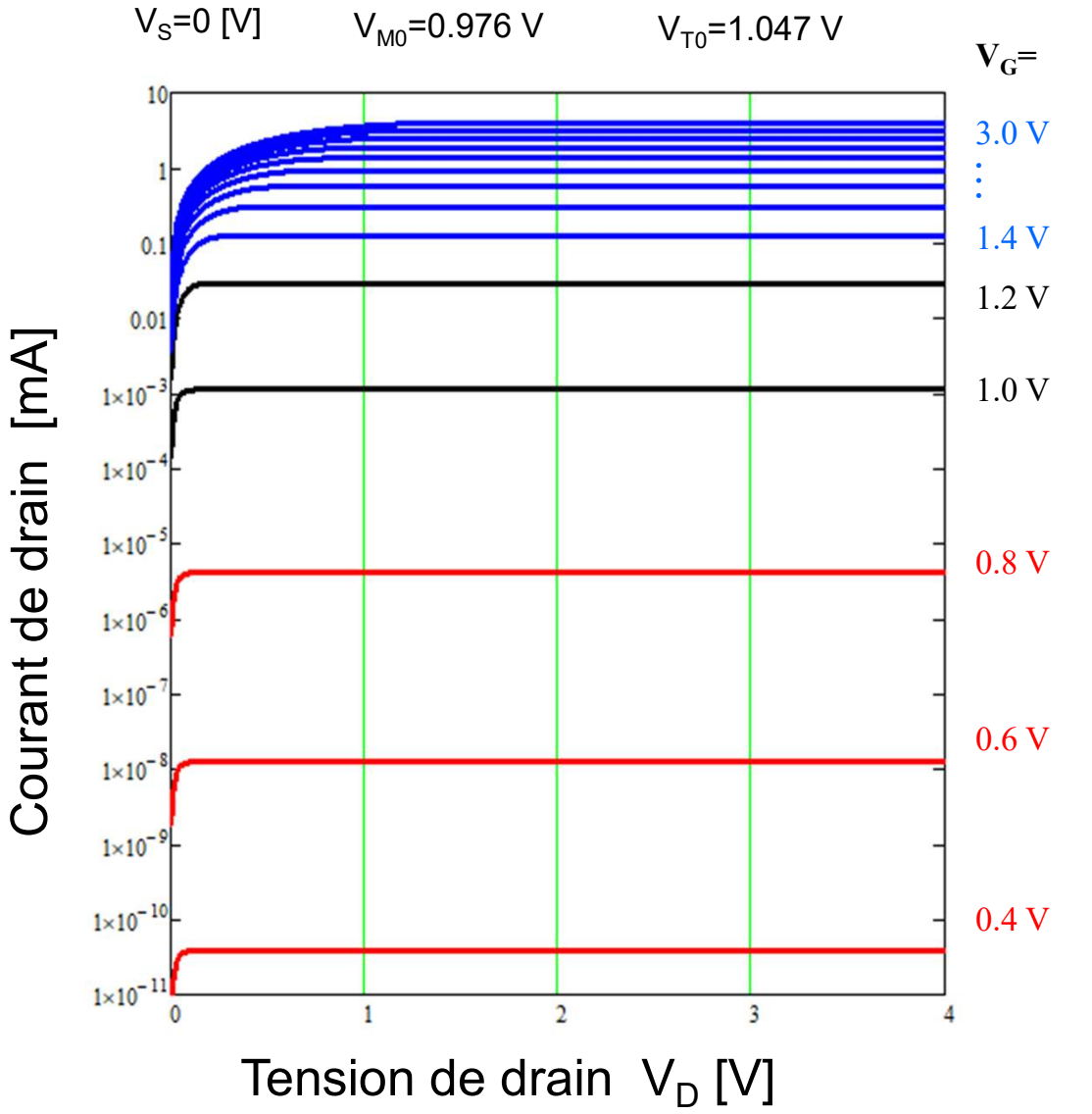




**Entrée sur la capacité de gate**
**→ $R_{in}$ infinie pour ω=0.**

# Avalanche breakdown



# Courant de drain: Modèle EKV




**Inversion forte**

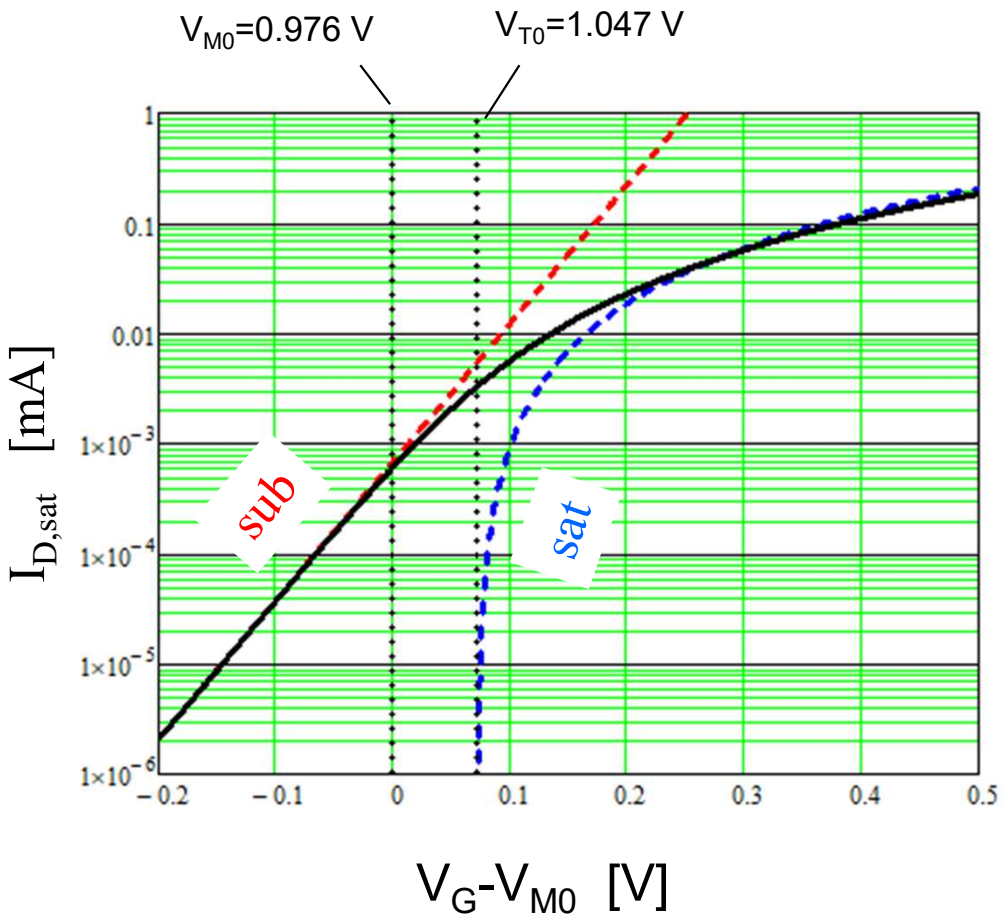
**Quadratique**

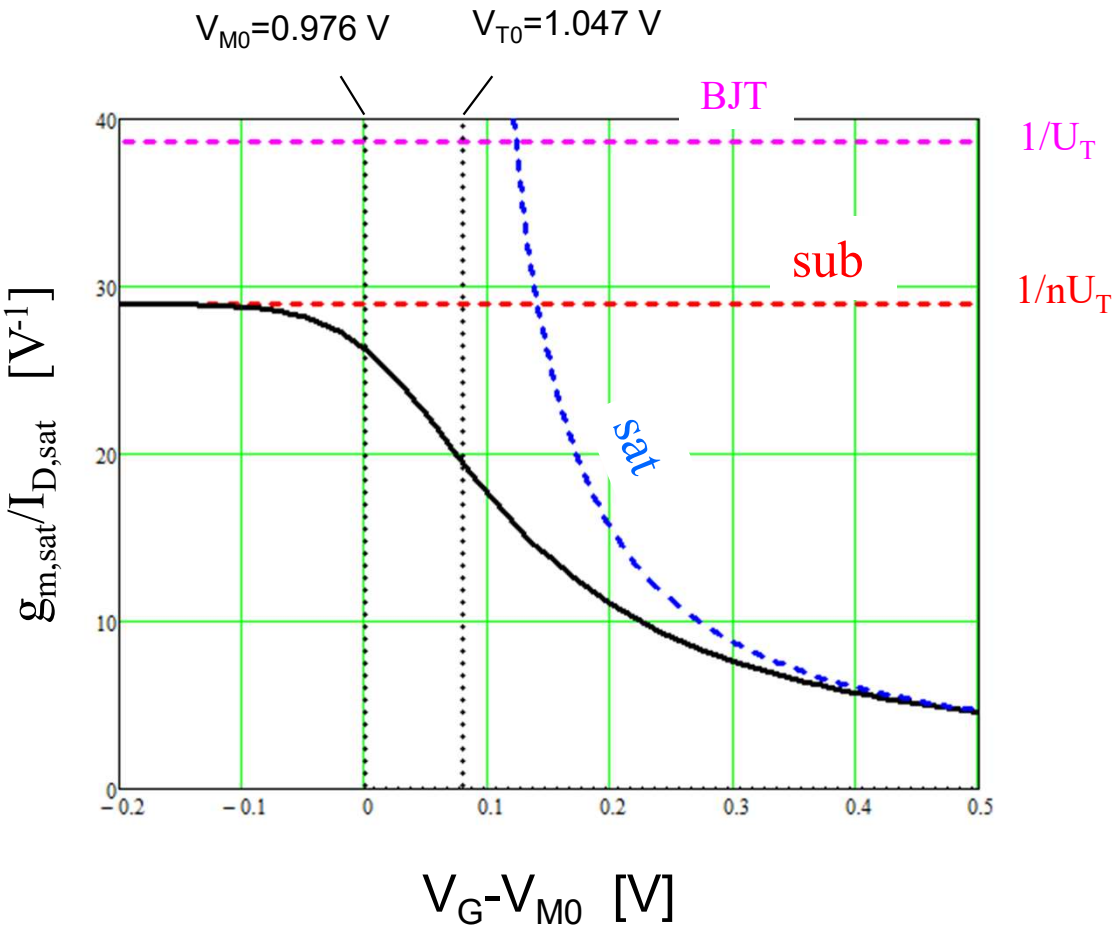
**Inversion modérée**

**Inversion faible «sub-threshold»**

**Exponentiel BJT**

# Comparaison des modèles



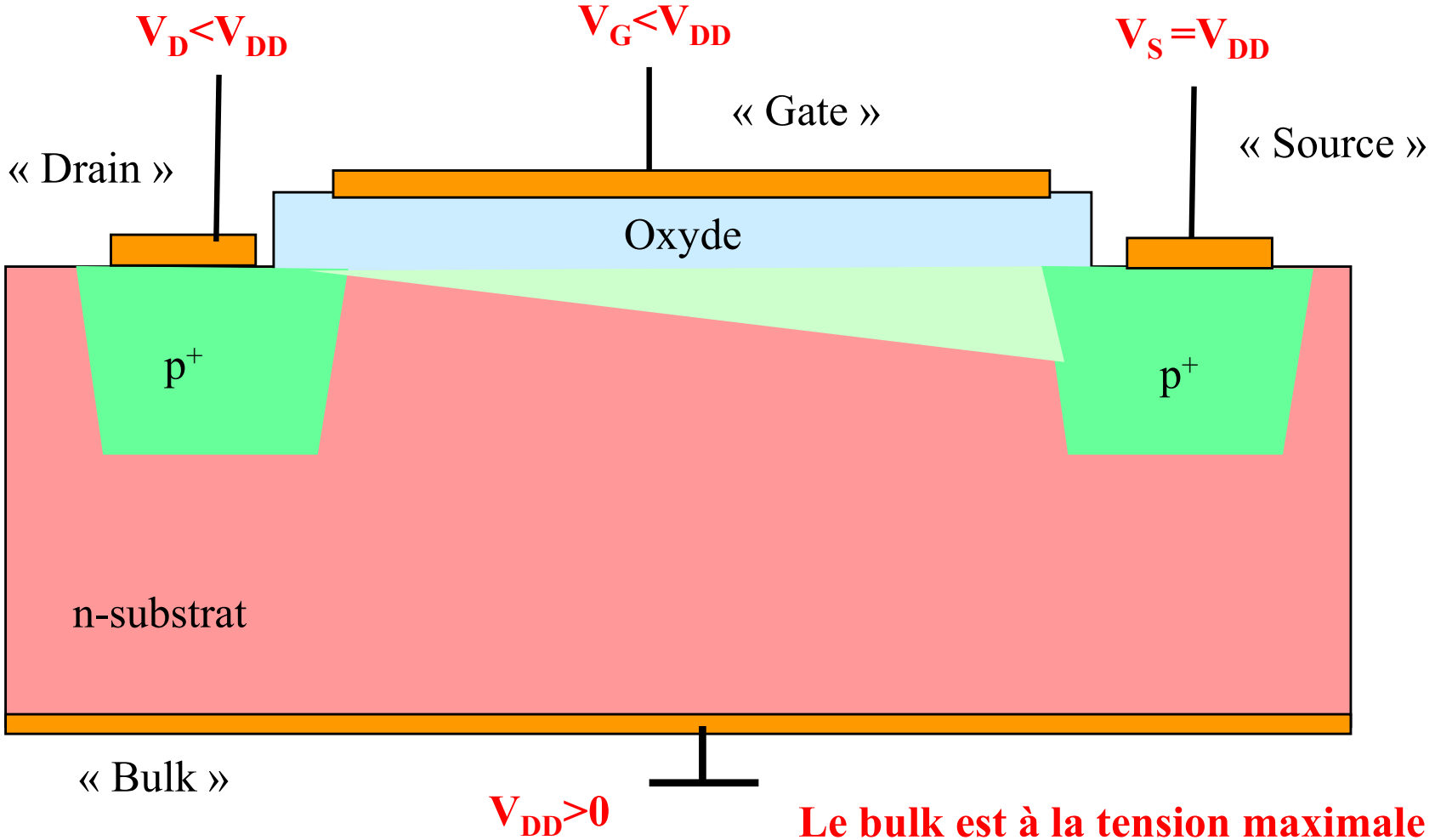

$C_{ox}$=3fF/um$^2$
W/L=10
T=300 K

$u_n$=1000cm$^2$/V.s
n=4/3

# PMOS: MOSFET à canal P

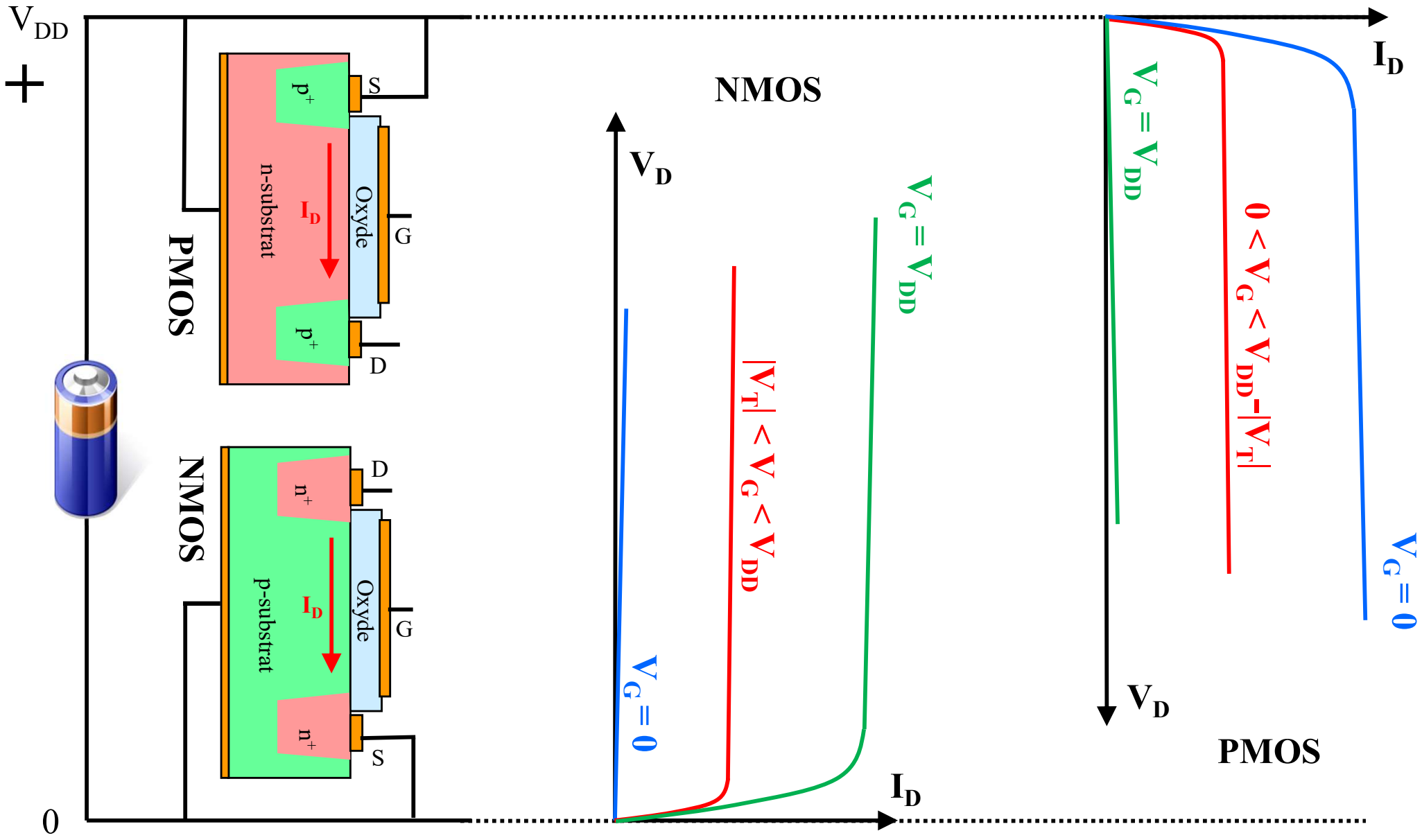
**Le drain et le gate sont à des tensions inférieures au bulk**

**La source est à la tension de bulk**




**Le bulk est à la tension maximale**

# Comparaison NMOS et PMOS: «Complémentarité»



# Exercice E10.2:
# VLSI et dissipation d'énergie

Considérons un chip avec une "Very Large Scale Integration" (VLSI) travaillant à température ambiante. Il contient $10^9$ NMOS, tous "fermés" donc avec une tension de gate $V_G$=0. Le courant "subthreshold" est exprimé par:

$$I_{D,sub} \cong I_{0,sub} \cdot e^{q(V_G - V_T)/nkT} \quad avec \quad n = 1.33$$

A) Le courant à $V_G$=0 V pour une tension de threshold $V_T$=0.5 V est de 4 pA par transistor. Quelle est la consommation en courant de tout le chip lorsque les transistors sont tous fermés ?

B) Nous diminuons la tension de threshold à $V_T$=0.25V. Quelle est maintenant la consommation en courant de tout le chip lorsque les transistors sont tous fermés ?

Commentaire: Cet exercice vise à montrer que le courant "subthreshold" pose une limite inférieure pour la tension de voltage, ceci afin d'assurer une bonne "fermeture" des transistors. Dans un micro-processeur, il y a en effet beaucoup plus de transistors au repos que de transistors "ouverts".

# Exercice E10.3: question de réflexion

Répondez à la question de réflexion

| | |
|---|---|
| | Quelles sont les contraintes sur l'oxyde d'une structure MOS ?<br><br>Discutez le cas d'une structure MOS sur substrat p en inversion forte (transistor) et celui de la même structure en déplétion profonde (CCD). |

Exemple: on applique 5V sur le gate. Dans lequel des deux cas (inversion forte ou déplétion profonde) le champ électrique dans l'oxyde est-il le plus important ? (risque de claquage!).

# Exercices E10.4

E10.4: MOSFET avec grille et drain court-circuités

a) Lorsque la tension de drain et celle de gate sont court-circuitées ($V_G$=$V_D$), comparez la tension de drain $V_D$ avec la tension de saturation $V_{D,sat}$. (nous supposons une tension de threshold $V_{M0}$ positive pour le NMOS, et la source et substrat connectés à la masse)

b) Que peut-on en déduire sur le régime de fonctionnement du NMOS ?

c) Déterminez la relation courant-tension de ce transistor NMOS avec la grille et le drain court-circuités.

d) Comment peut-on à partir de la mesure de cette caractéristique déterminer la tension de seuil ?